RFIC Design and Testing for Wireless Communications

A Full-Day Tutorial at VLSI Design & Test Symposium
July 23, 2008

Lecture 1: Introduction

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Abstract

This tutorial discusses design and testing of RF integrated circuits (RFIC). It is suitable for engineers who plan work on RFIC but did not have training in that area, those who work on IC design and wish to sharpen their understanding of modern RFIC design and test methods, and engineering managers. It is an abbreviated version of a one-semester university course. Specific topics include semiconductor technologies for RF circuits used in a wireless communications system; basic characteristics of RF devices – linearity, noise figure, gain; RF front-end design – LNA, mixer; frequency synthesizer design – phase locked loop (PLL), voltage controlled oscillator (VCO); concepts of analog, mixed signal and RF testing and built-in self-test; distortion – theory, measurements, test; noise – theory, measurements, test; RFIC SOCs and their testing.

Objectives

- To acquire introductory knowledge about integrated circuits (IC) used in radio frequency (RF) communications systems.
- To learn basic concept of design of RFIC.
- To learn basic concepts of RFIC testing.

Outline

- Introduction to VLSI devices used in RF communications
  - SOC and SIP
  - Functional components
  - Technologies
- Design concepts
- Test concepts
  - Basic RF measurements
  - Distortion characteristics
  - Noise
  - SOC testing and built-in self-test (BIST)

References

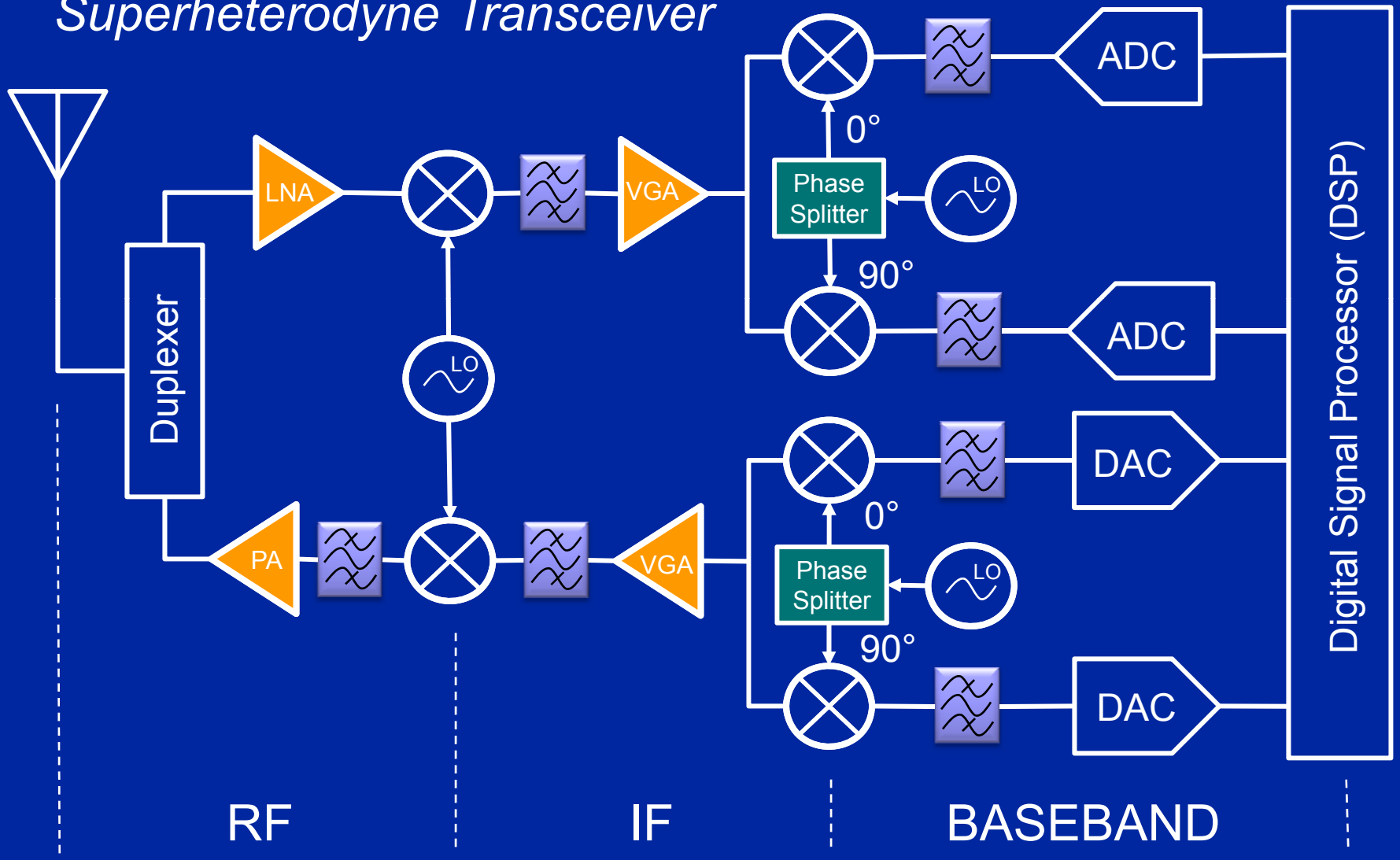
1. **M. L. Bushnell and V. D. Agrawal**, *Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits*, **Boston: Springer, 2000.**
2. **J. Kelly and M. Engelhardt**, *Advanced Production Testing of RF, SoC, and SiP Devices*, **Boston: Artech House, 2007.**
3. **B. Razavi**, *RF Microelectronics*, **Upper Saddle River, New Jersey: Prentice Hall PTR, 1998.**
4. **J. Rogers, C. Plett and F. Dai**, *Integrated Circuit Design for High-Speed Frequency Synthesis*, **Boston: Artech House, 2006.**
5. **K. B. Schaub and J. Kelly**, *Production Testing of RF and System-on-a-chip Devices for Wireless Communications*, **Boston: Artech House, 2004.**

Schedule

09:30AM – 10:00AM	Lecture 1	Introduction	Agrawal
10:00AM – 11:00AM	Lecture 2	RF Design I	Dai
11:00AM – 11:30AM	Break		
11:30AM – 13:00PM	Lecture 3	RF Design II	Dai
13:00PM – 14:00PM	Lunch		
14:00PM – 15:00PM	Lectures 4	RF Testing I	Agrawal
15:00PM – 15:30PM	Break		
15:30PM – 17:30PM	Lectures 5-7	RF Testing II	Agrawal
	Lecture 8	RF BIST	Dai

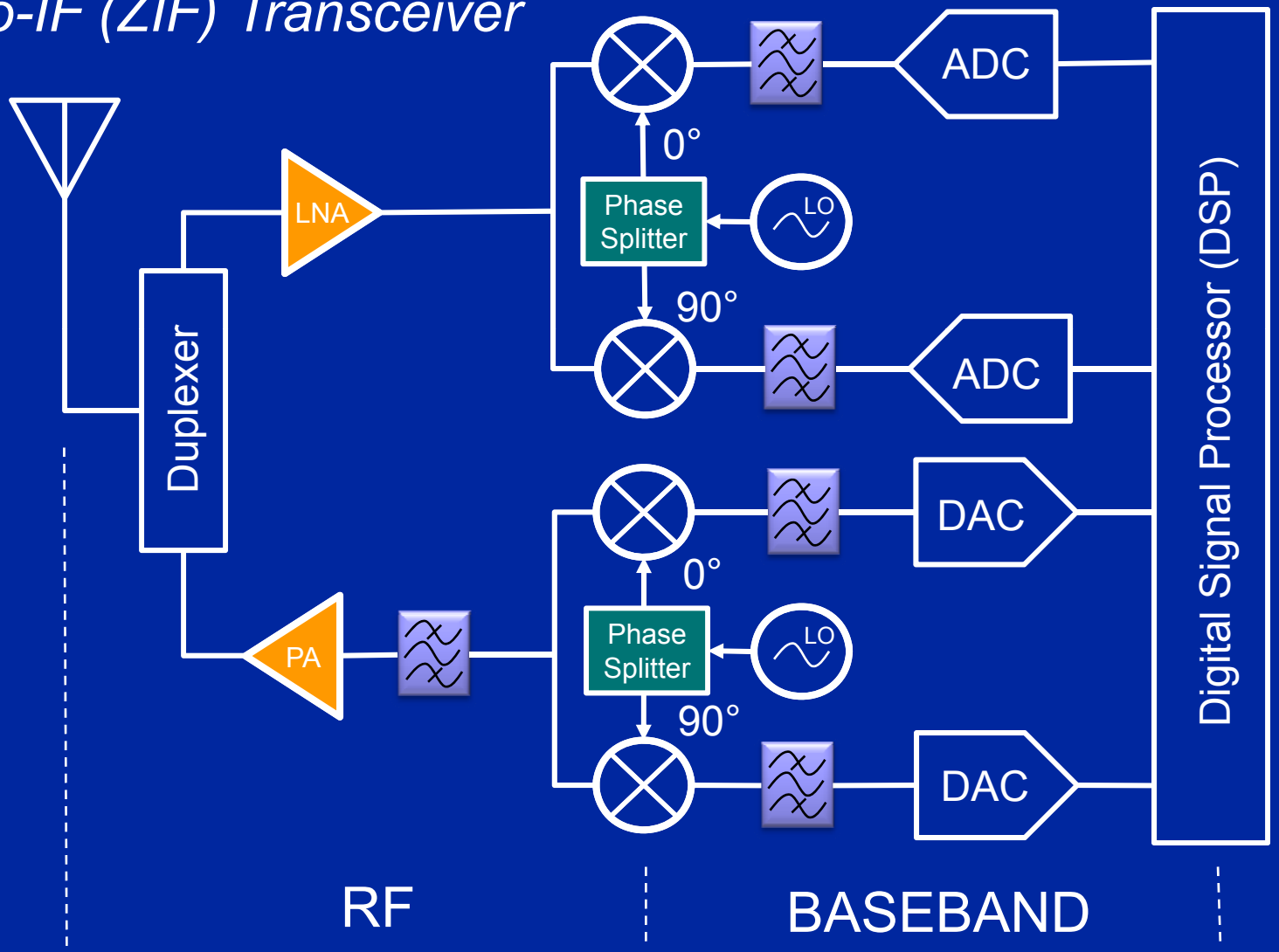
An RF Communications System

Superheterodyne Transceiver



An Alternative RF Communications System

Zero-IF (ZIF) Transceiver

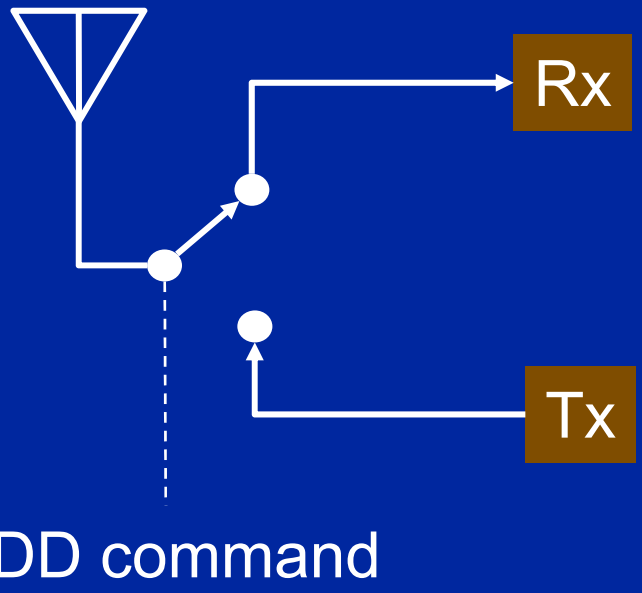


Components of an RF System

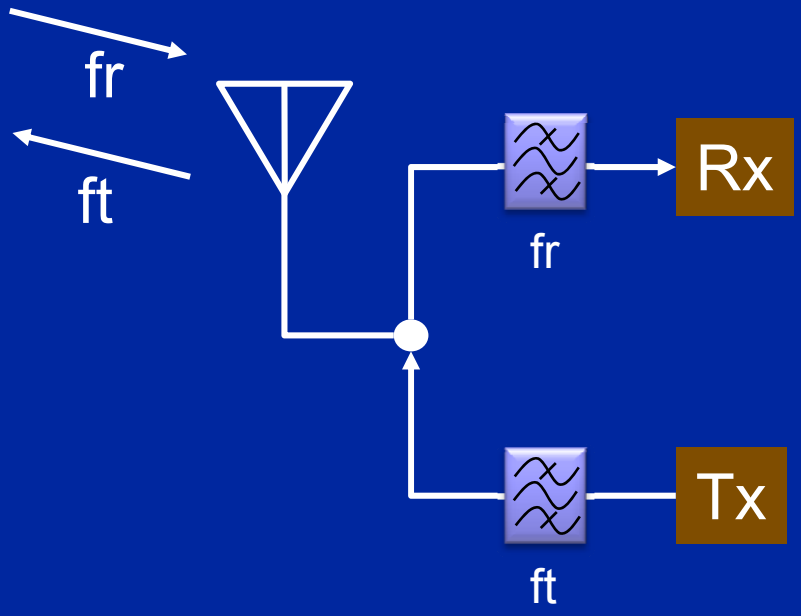
- **Radio frequency**
  - Duplexer
  - LNA: Low noise amplifier
  - PA: Power amplifier
  - RF mixer
  - Local oscillator
  - Filter
- **Intermediate frequency**
  - VGA: Variable gain amplifier
  - Modulator
  - Demodulator
  - Filter
- **Mixed-signal**
  - ADC: Analog to digital converter
  - DAC: Digital to analog converter
- **Digital**
  - Digital signal processor (DSP)

Duplexer

- **TDD: Time-Division Duplexing**
  - Same Tx and Rx frequency
  - RF switch (PIN or GaAs FET)
  - Less than 1dB loss



- **FDD: Frequency-Division Duplexing**
  - Tx to Rx coupling (-50dB)
  - More loss (3dB) than TDD
  - Adjacent channel leakage



LNA: Low Noise Amplifier

- Amplifies received RF signal
- Typical characteristics:
  - Noise figure 2dB
  - IP3 – 10dBm
  - Gain 15dB
  - Input and output impedance 50Ω
  - Reverse isolation 20dB
  - Stability factor > 1
- Technologies:
  - Bipolar
  - CMOS
- Reference: Razavi, Chapter 6.

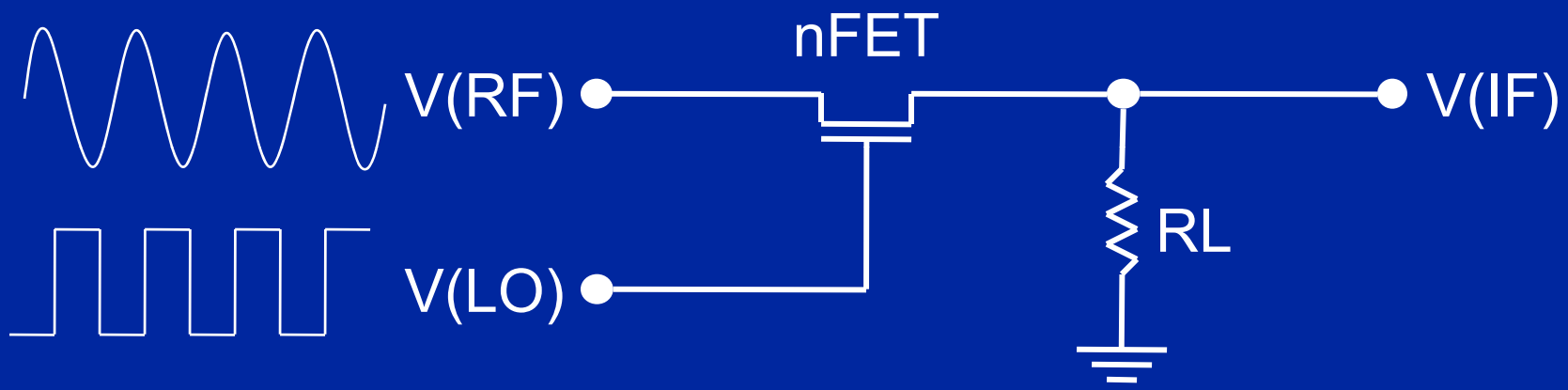
PA: Power Amplifier

- Feeds RF signal to antenna for transmission
- Typical characteristics:
  - Output power: +20 to +30 dBm
  - Efficiency: 30% to 60%
  - IMD: – 30dBc
  - Supply voltage: 3.8 to 5.8 V
  - Gain: 20 to 30 dB
  - Output harmonics: – 50 to – 70 dBc
  - Power control: On-off or 1-dB steps
  - Stability factor: > 1
- Technologies:
  - GaAs
  - SiGe
- Reference: Razavi, Chapter 9.

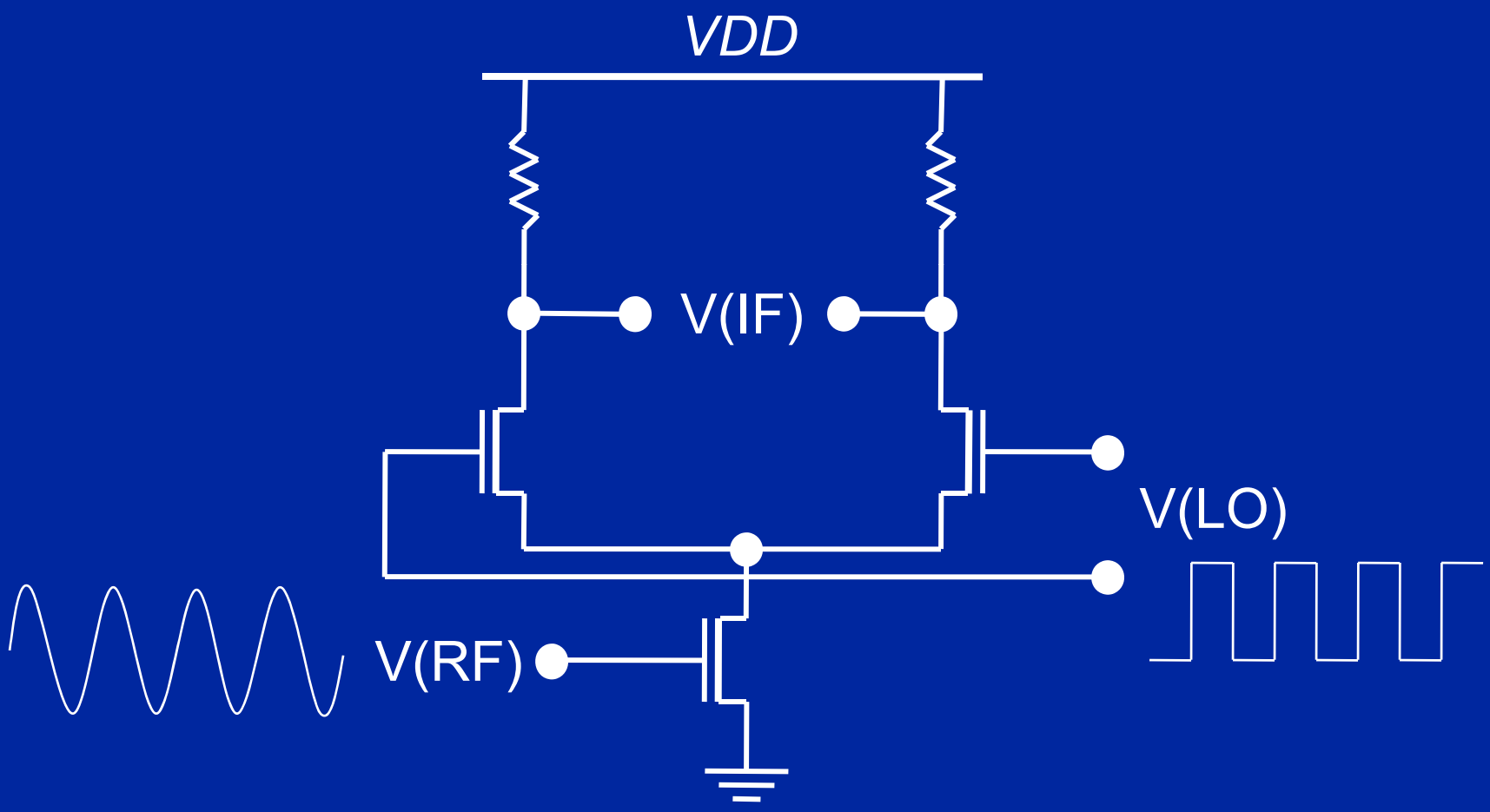
Mixer or Frequency (Up/Down) Converter

- Translates frequency by adding or subtracting local oscillator (LO) frequency
- Typical characteristics:
  - Noise figure 12dB
  - IP3 +5dBm
  - Gain 10dB
  - Input impedance 50Ω
  - Port to port isolation 10-20dB
- Tecnologies:
  - Bipolar
  - MOS
- Reference: Razavi, Chapter 6.

Passive Mixer



Active Mixer

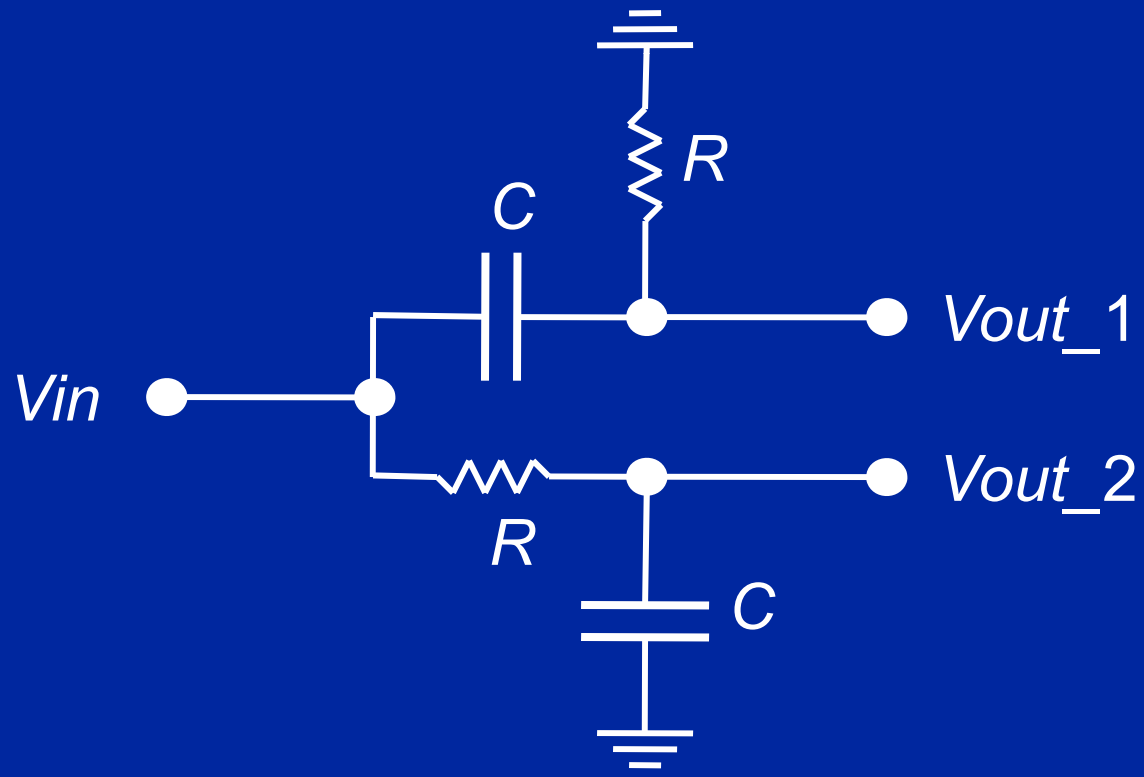


LO: Local Oscillator

- Provides signal to mixer for down conversion or upconversion.
- Implementations:
  - Tuned feedback amplifier
  - Ring oscillator
  - Phase-locked loop (PLL)
  - Direct digital synthesizer (DDS)

Phase Splitter

- Splits input signal into two same frequency outputs that differ in phase by 90 degrees.
- Used for image rejection.



SOC: System-on-a-Chip

- All components of a system are implemented on the same VLSI chip.
- Requires same technology (usually CMOS) used for all components.
- Components not implemented on present-day SOC:
  - Antenna
  - Power amplifier (PA)

SIP: System-in- Package

- Several chips or SOC are included in a package.
- Routing within SIP may be provided via a semiconductor substrate.
- RF communications system may contain:
  - SIP, containing
    - SOC consisting of
      - CMOS digital and mixed-signal components (DSP, ADC, DAC)
      - CMOS LNA and mixers
      - CMOS DDS
      - Filters
  - Power amplifier (PA)
  - Antenna

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Lecture 2: RF Design I

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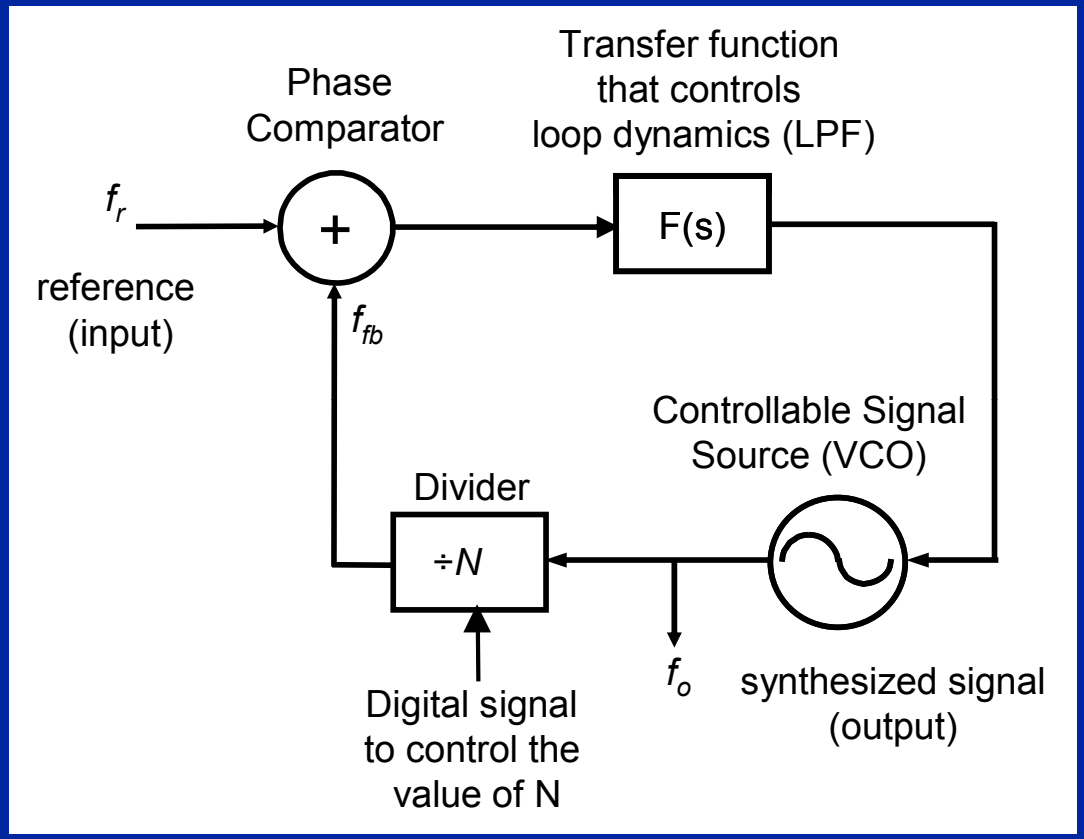
Phase Lock Loop Integer-N Frequency Synthesizer



$$f_o = N \cdot f_{\text{ref}}$$

N is an integer → the minimum step size = f_r →to get a smaller step size, the reference frequency must be made smaller → N must be higher in order to generate the same f_o → larger phase noise (in-band noise magnified 20logN times by the loop).

Fractional-N Concept

If the loop divisor *N* is a fractional number, e.g., N=K/F, where K and F are integer numbers → the minimum step size = f_r /F→ can achieve small step size without lowering the reference frequency → loop divisor N can be small in order to generate the same f_o → better phase noise (in-band noise magnified 20logN times by the loop).

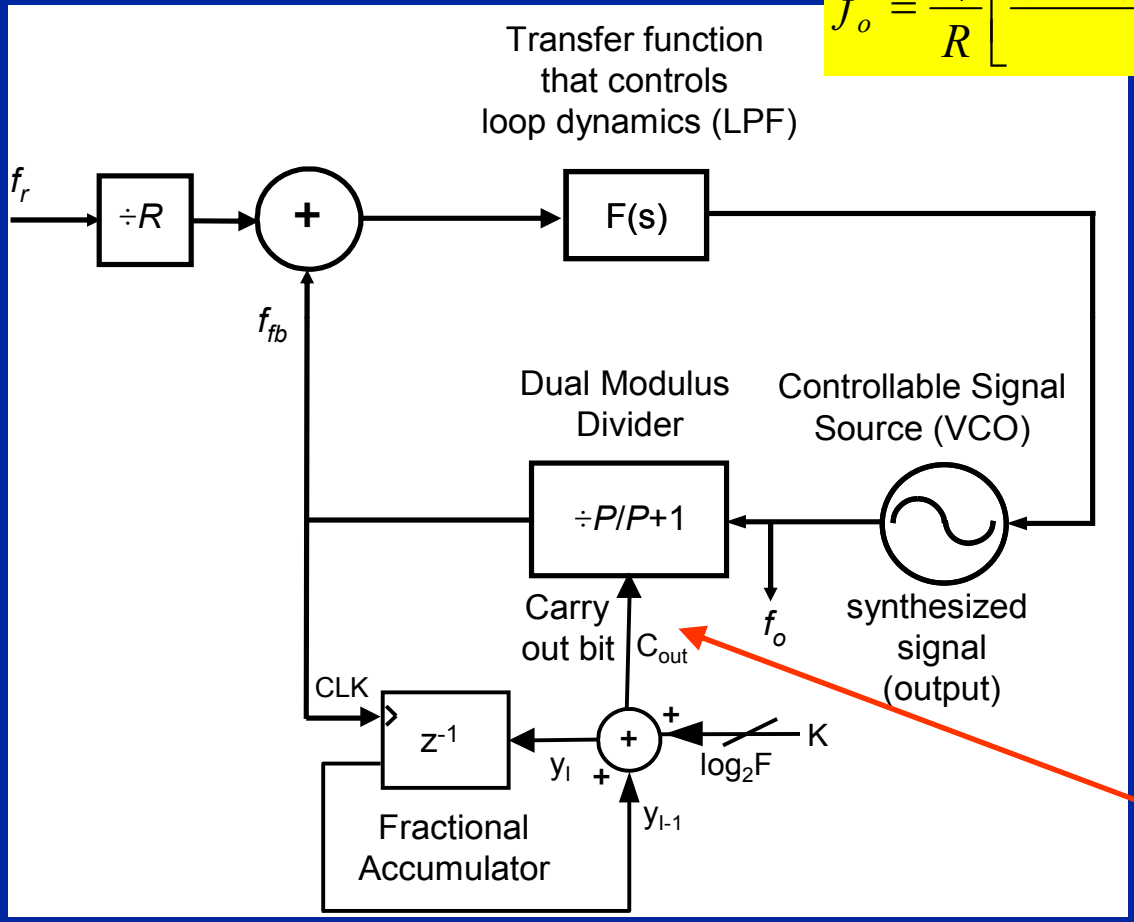
How can we design a fractional divider? Divider is a digital block and its output transits only at the input clock edge → we can only generate integer frequency divider!!

Dual-modulus divider P/P+1: by toggling between the two integer division ratios, a fractional division ratio can be achieved by time-averaging the divider output. As an example, if the control changes the division ratio between 8 and 9, and the divider divides by 8 for 9 cycles and by 9 for 1 cycle and then the process repeats itself, then the average division ratio will be:

$$\overline{N} = \frac{8 \times 9 + 9 \times 1}{10} = 8.1$$

Fractional-N Synthesizer with a Dual Modulus Prescaler

$$f_o = \frac{f_r}{R}\left[\frac{(P+1)K + P(F-K)}{F}\right] = \frac{f_r}{R}\left[P + \frac{K}{F}\right]$$



$$\text{Step Size} = \frac{f_r}{RF}$$

$$f_{C_{out}} = \frac{Kf_{clk}}{F}$$

Fractional Accumulator Operations

$$f_{C_{\text{out}}} = \frac{Kf_{clk}}{F}$$

Accumulator operations with $F = 8$, $K = 1$

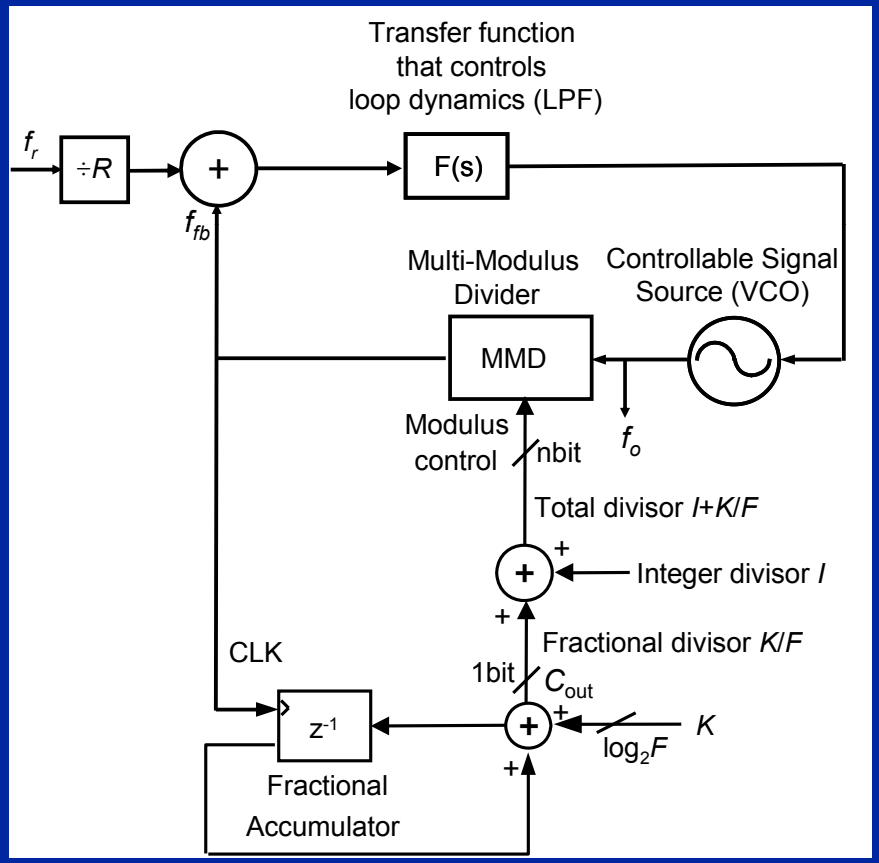
clock cycle i	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
y_i	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2
y_{i-1}	NA	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1
C_{out}	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0

Accumulator operations with $F = 8$, $K = 3$

clock cycle i	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
y_i	0	3	6	1	4	7	2	5	0	3	6	1	4	7	2	5	0	3	6
y_{i-1}	NA	0	3	6	1	4	7	2	5	0	3	6	1	4	7	2	5	0	3
C_{out}	1	0	0	1	0	0	1	0	1	0	0	1	0	0	1	0	1	0	0

Fractional-N Frequency Synthesizer with a Multi-Modulus Divider

$$N_{\text{MMD}} = P_1 + 2^1 P_2 + \ldots 2^{n-2} P_{n-1} + 2^{n-1} P_n + 2^n$$

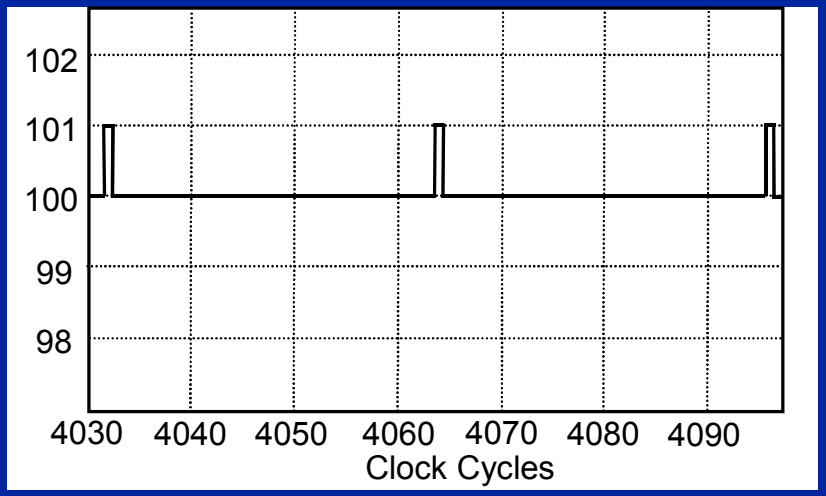


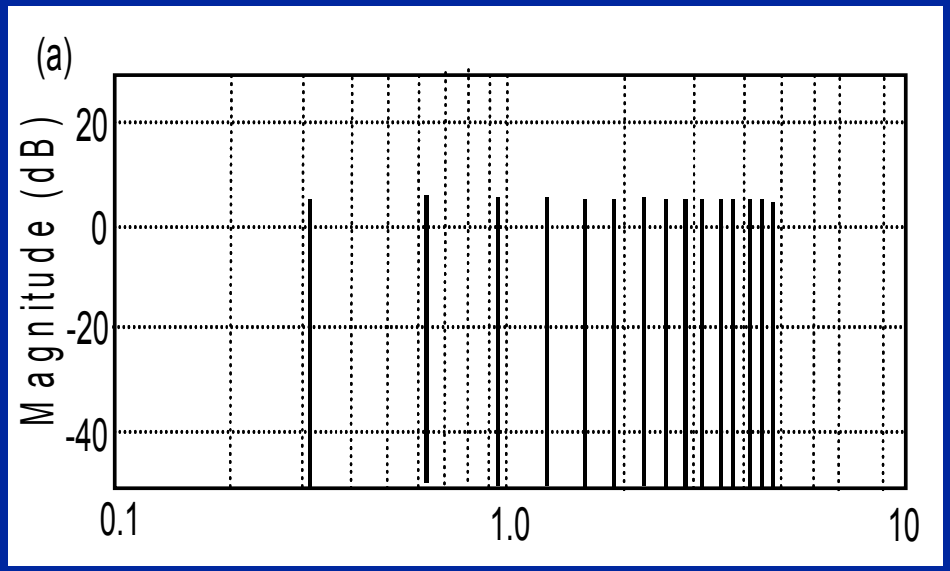
$$f_o = \frac{f_r}{R}\left[I + \frac{K}{F}\right]$$

Fractional-*N* Spurious Components

Any repeatable pattern in the time domain causes spurious tones in the frequency domain.

The fractional accumulator periodically generates the carry out that toggles the loop division ratio → spurious tones at multiples of the carryout frequency $f_r \cdot (K/F)$, which is the step size of the fractional-N synthesizer. → the smaller the step size is, the closer the spur locates to the carrier.





Design a Fractional-*N* Synthesizer Architecture

for synthesizing 11 channels from 819.2 MHz to 820.96 MHz with a step size of 160 kHz and reference comparison frequency of f_r/R=5.12 MHz. Determine the frequencies of fractional-*N* spurious components.

Solution: The synthesizer step size is given by

$$\frac{f_r}{R}\cdot\frac{1}{F}=160\ \text{kHz}$$

Since the comparison frequency is f_r/R = 5.12 MHz, the fractional accumulator size can be chosen as:

$$F=\frac{f_r}{R}\cdot\frac{1}{160\text{kHz}}=\frac{5120\text{kHz}}{160\text{kHz}}=32$$

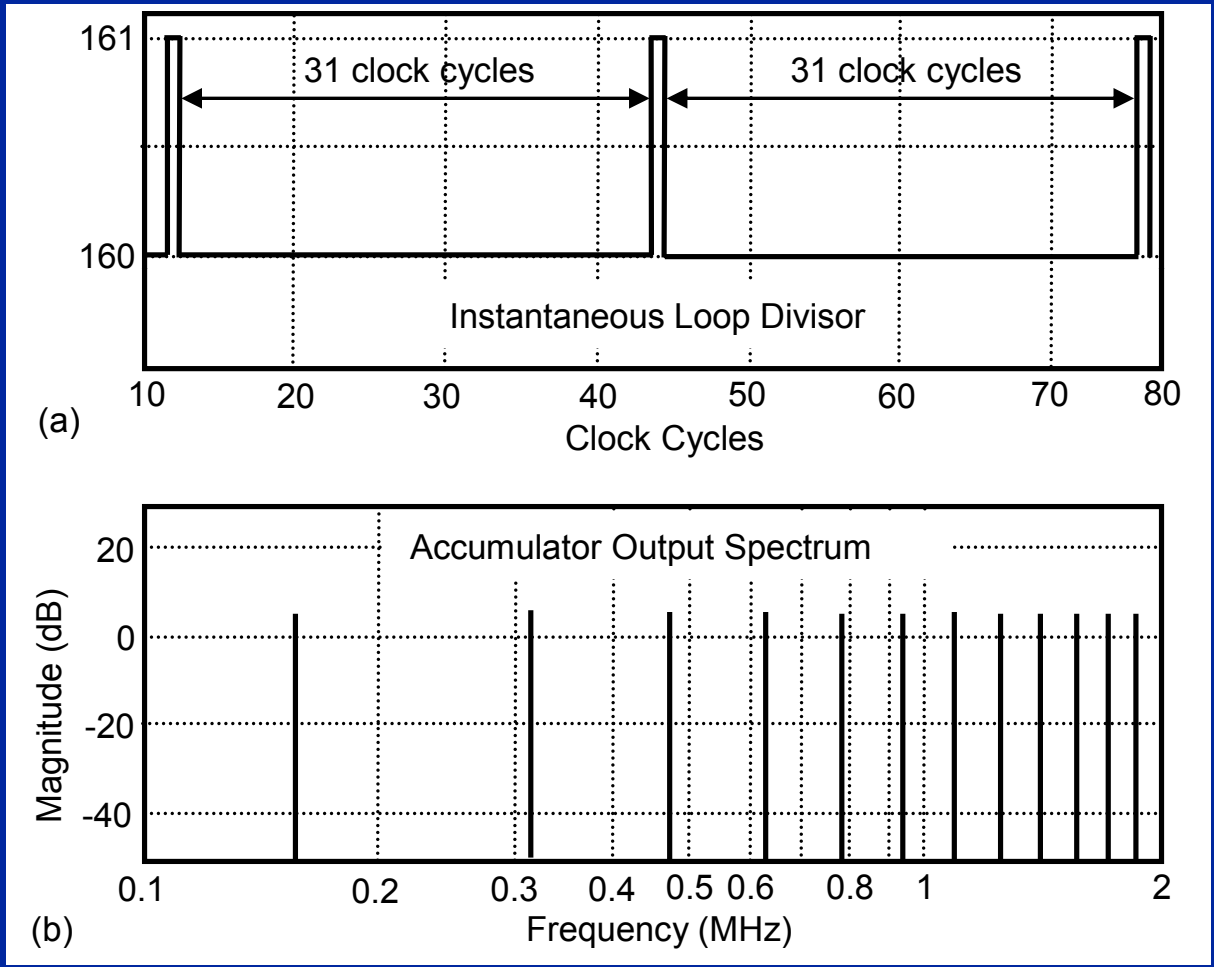
which can be implemented using a 5-bit accumulator. The accumulator input, i.e., the fine tune frequency word *K*, can be programmed from 0 to 10 to cover the 11 channels from 819.2 MHz to 820.96 MHz with step size of 160 kHz (the first channel does not require any fractionality). The integer divisor ratio, i.e., the coarse tune frequency word *I*, can be determined by the channel frequency. For instance, the first channel frequency is synthesized as:

$$\frac{f_r}{R}\left(I+\frac{0}{F}\right)=\frac{f_r}{R}\cdot I=819.2\ \text{MHz}$$

which leads to *I* = 160. Hence, the loop total divisor is given by *N* = 160 + *K*/32, where *K* = 0, 1, … 10.

Simulated Fractional Accumulator Output

Loop divisor N = 160 + 1/32 and the comparison frequency fr/R = 5.12 MHz



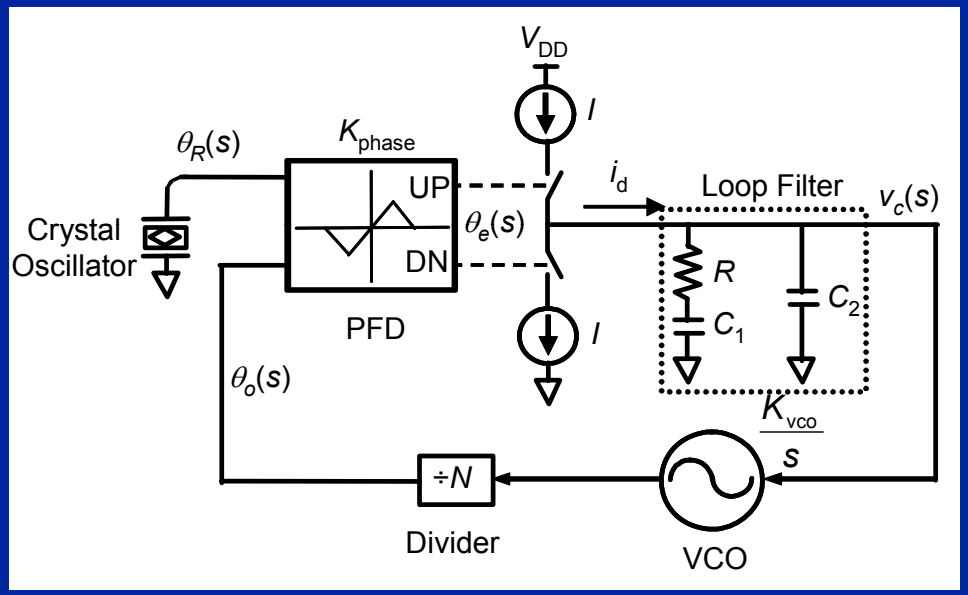
PLL Frequency Synthesizer

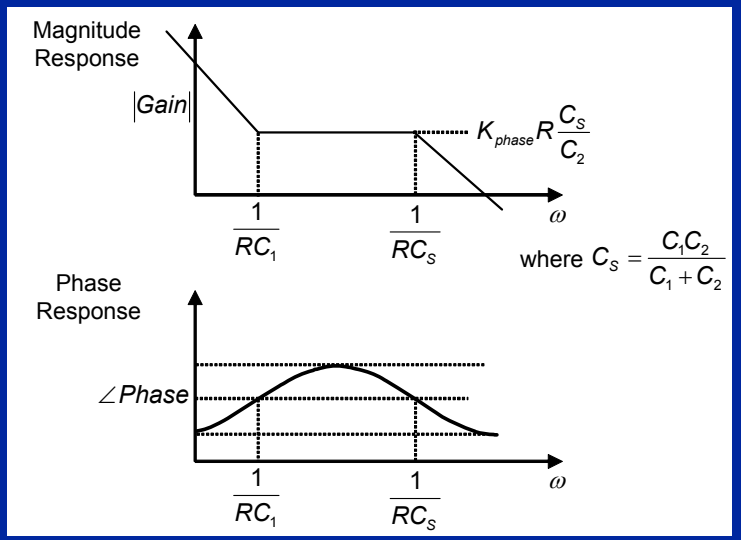
$$v_e(s) = K_{\mathrm{PD}}(\theta_R - \theta_o)$$

$$i_d = K_{CP}K_{PD}(\theta_R - \theta_o)$$

$$v_c = \frac{K_{\mathrm{PD}}K_{\mathrm{CP}}(\theta_R - \theta_o)(1+sC_1R)}{s(C_1+C_2)(1+sC_sR)}$$

$$C_s = \frac{C_1C_2}{C_1+C_2}$$





$$\frac{\theta_o}{v_c} = \frac{1}{N}\cdot\frac{K_{\mathrm{VCO}}}{s}$$

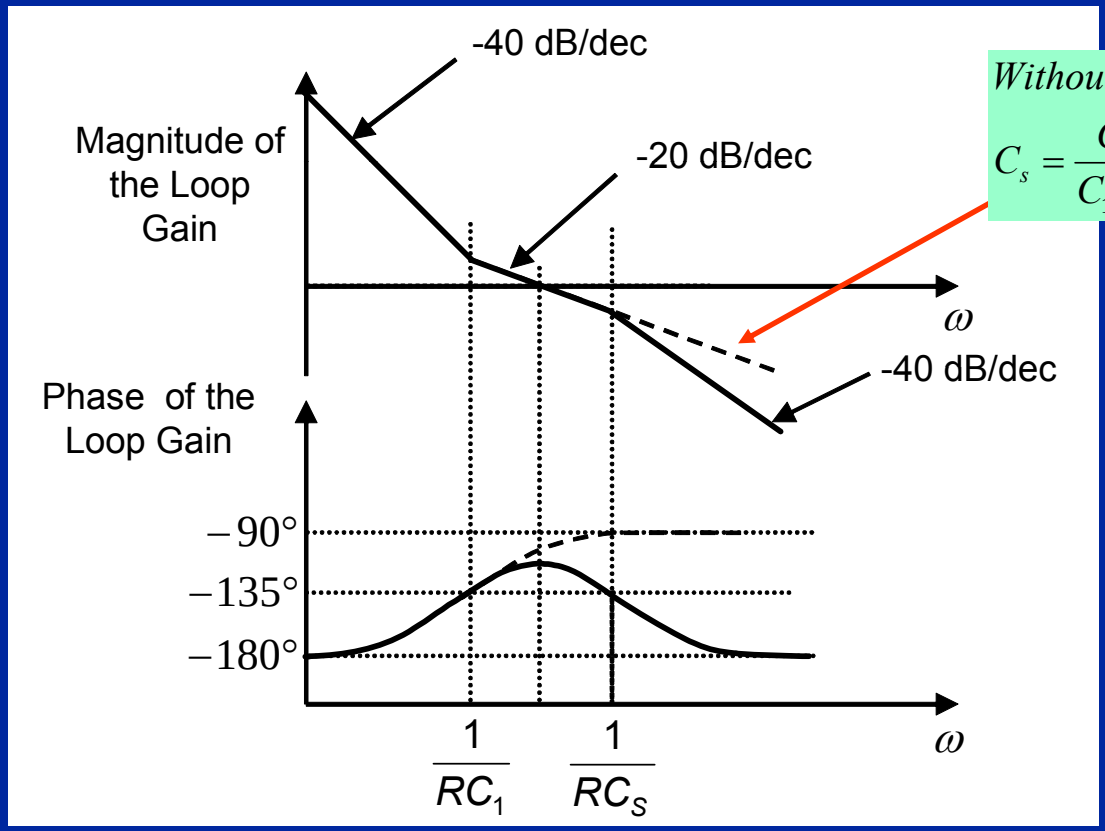
$$\frac{\theta_{\mathrm{VCO}}(s)}{v_c(s)} = \frac{K_{\mathrm{VCO}}}{s}$$

$$\omega_{\mathrm{VCO}} = K_{\mathrm{VCO}}v_c$$

Open Loop Transfer Function

$$\left(\frac{\theta_o}{\theta_R}\right)_{\text{open loop}} = \frac{K_{VCO}K_{PD}K_{CP}(1+sC_1R)}{s^2N(C_1+C_2)(1+sC_sR)}$$

C_2 (about $C_1/10$) adds a high frequency pole to clean up high frequency ripple on the control line.



Without C_2,

$$C_s = \frac{C_1C_2}{C_1+C_2} = 0$$

Closed Loop Transfer Function

$$\frac{\theta_o}{\theta_R} = \frac{K_{VCO}K_{PD}K_{CP}(1+sC_1R)}{s^2N(C_1+C_2)(1+sC_sR)+K_{VCO}K_{PD}K_{CP}(1+sC_1R)}$$

$2nd-orderPLL$
$Without\ C_2, C_s = 0$

$$\frac{\theta_o}{\theta_R} = \frac{K_{VCO}K_{PD}K_{CP}(1+sC_1R)}{s^2NC_1+K_{VCO}K_{PD}K_{CP}(1+sC_1R)}$$

natural frequency

$$\omega_n = \sqrt{\frac{K}{NC_1}}$$

$$\frac{\theta_o}{\theta_R} = \frac{\omega_n^2\left(\frac{2\zeta}{\omega_n}s+1\right)}{s^2+2\zeta\omega_n s+\omega_n^2}$$

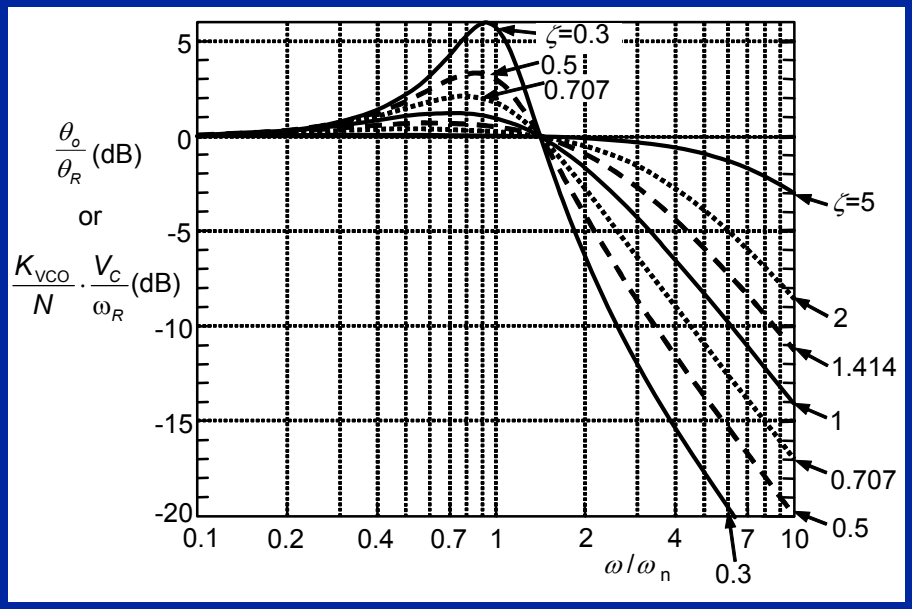
damping constant

$$\zeta = \frac{R}{2}\sqrt{\frac{KC_1}{N}}$$

$$\omega_{3dB} = \omega_n\sqrt{1+2\zeta^2+\sqrt{4\zeta^4+4\zeta^2+2}}$$

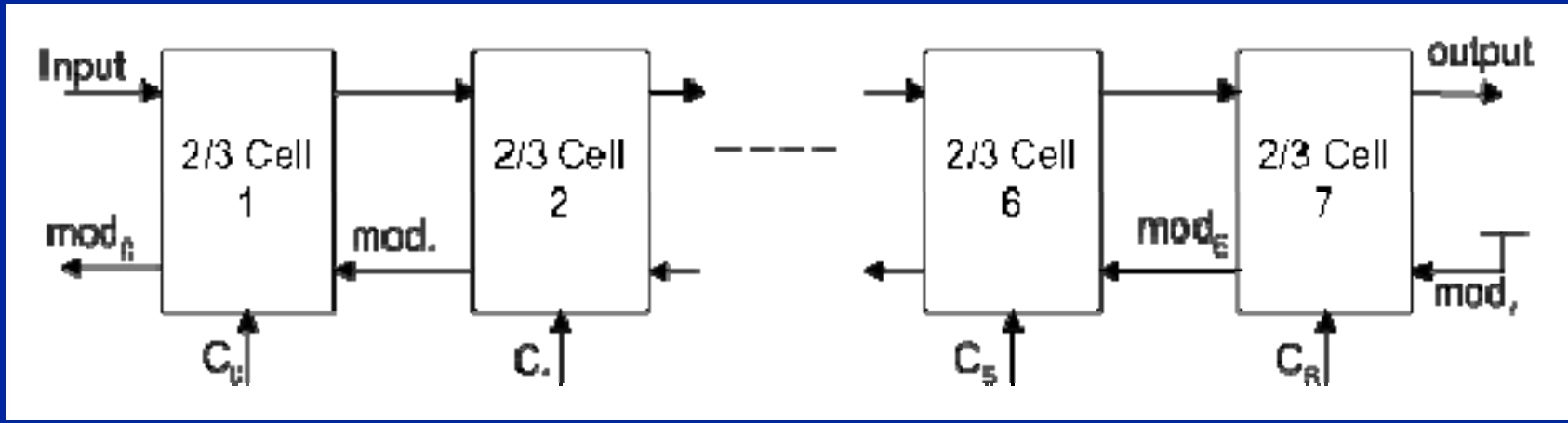
$$\omega_{3dB} \approx (1+\zeta\sqrt{2})\omega_n \quad \zeta < 1.5$$

$$\omega_{3dB} \approx 2\zeta\omega_n = K/N \quad \zeta > 1.5$$



PLL frequency response

MMD Architecture Using 2/3 Cells



$$N_{MMD} = 2^n + 2^{n-1}C_{n-1} + 2^{n-2}C_{n-2} + \cdots + 2C_1 + C_0$$

For 3 bit MMD, $N_{MMD}(n=3) = 8 + 4C_2 + 2C_1 + C_0 = 8 \sim 15$

Say, we need an MMD with division ratios: 128-135.

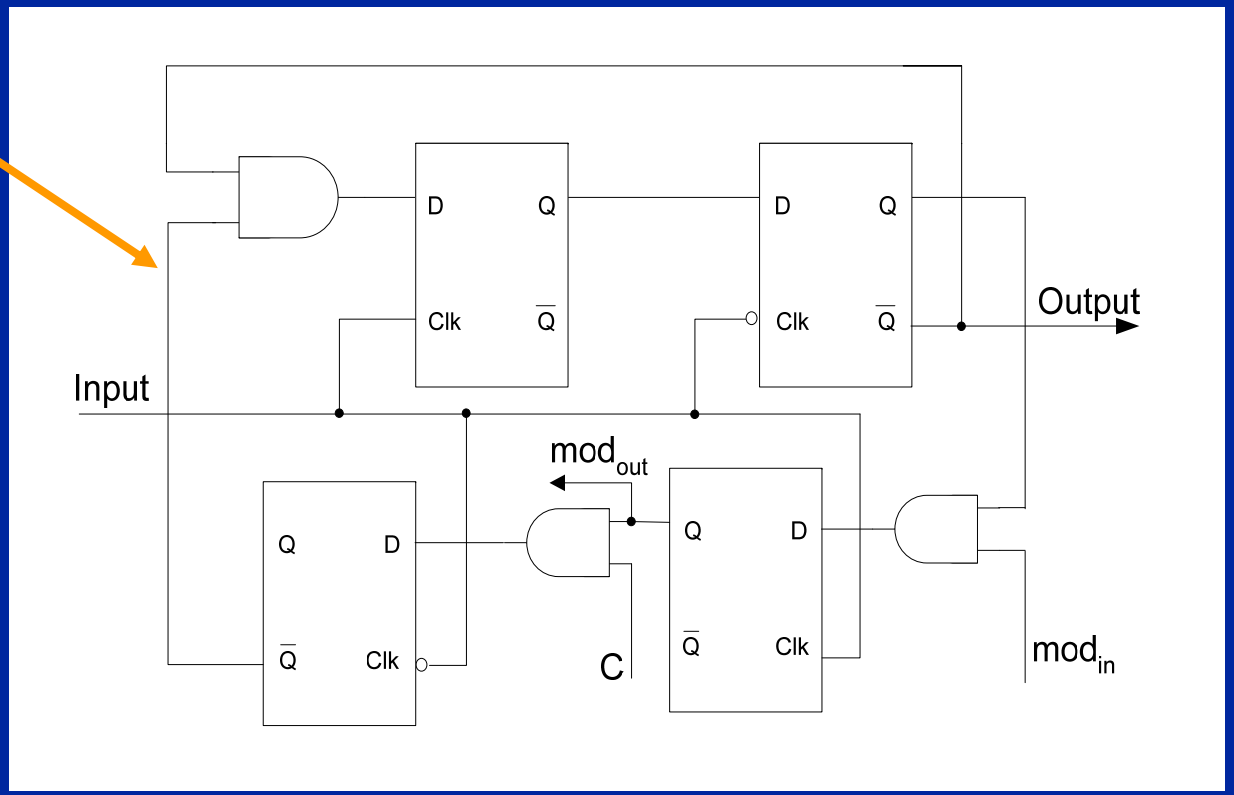
$$N = 2^7 + 2^6C_6 + 2^5C_5 + 2^4C_4 + 2^3C_3 + 2^2C_2 + 2^1C_1 + C_0$$

The division ratios obtained using 2/3 cells: 128-255.

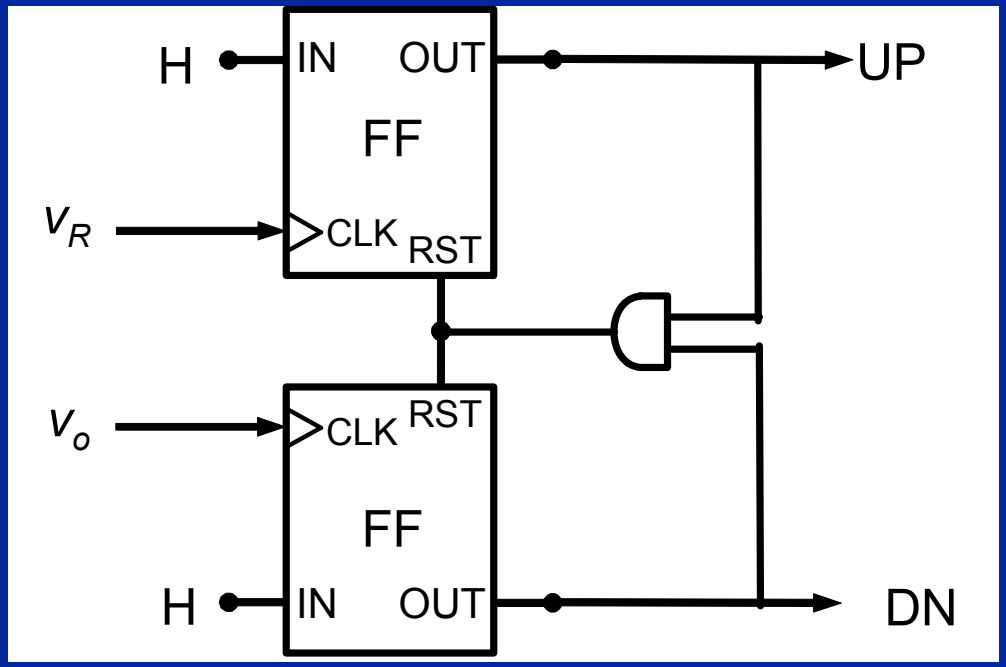
Dual Modulus Prescaler – 2/3 Cell

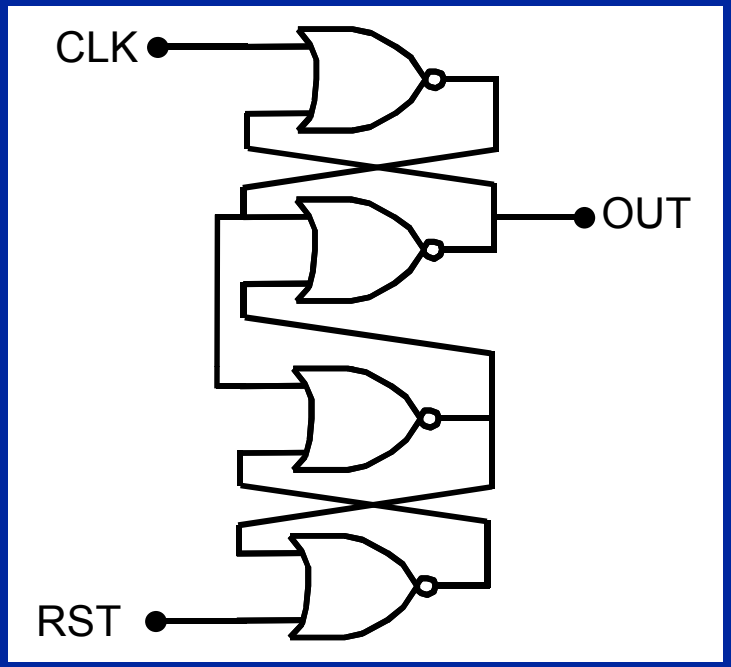
mod_{in}=1 and C=1 → F_o/F_{in}=1/3; mod_{in}=1 and C=0 → F_o/F_{in}=1/2
mod_{in}=0 and p=x → F_o/F_{in}=1/2

Dual modulus control



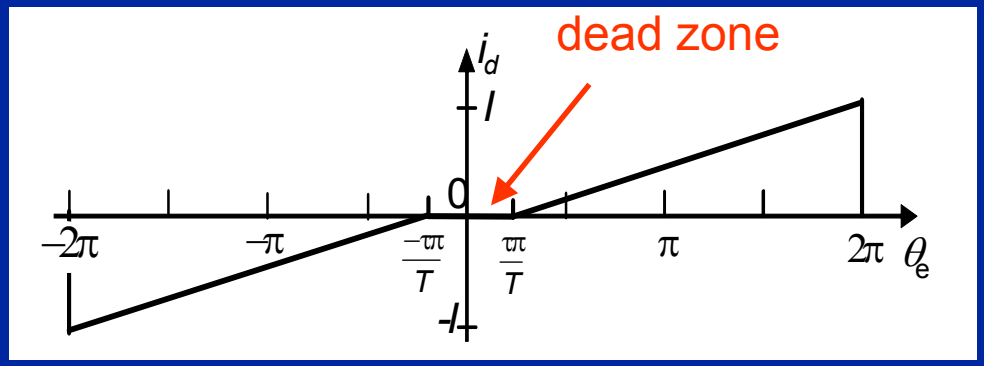
Tri-State PFD Circuit

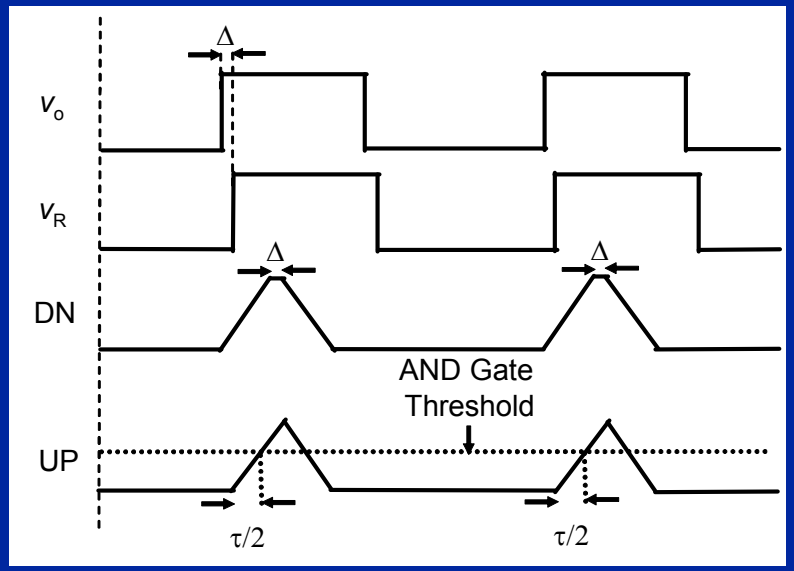


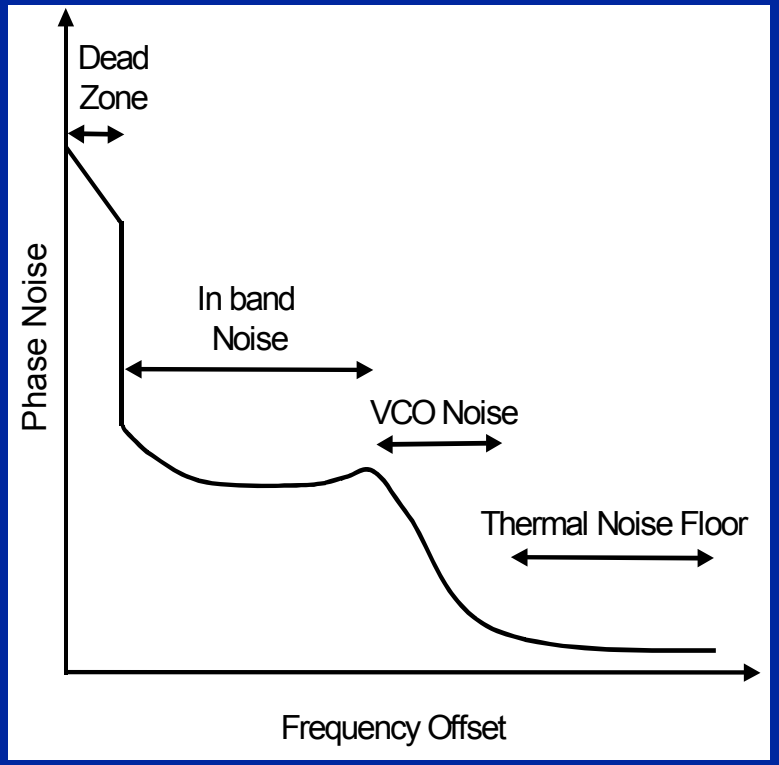


Positive edge-triggered D flip-flop with active low reset and hidden *D*=1

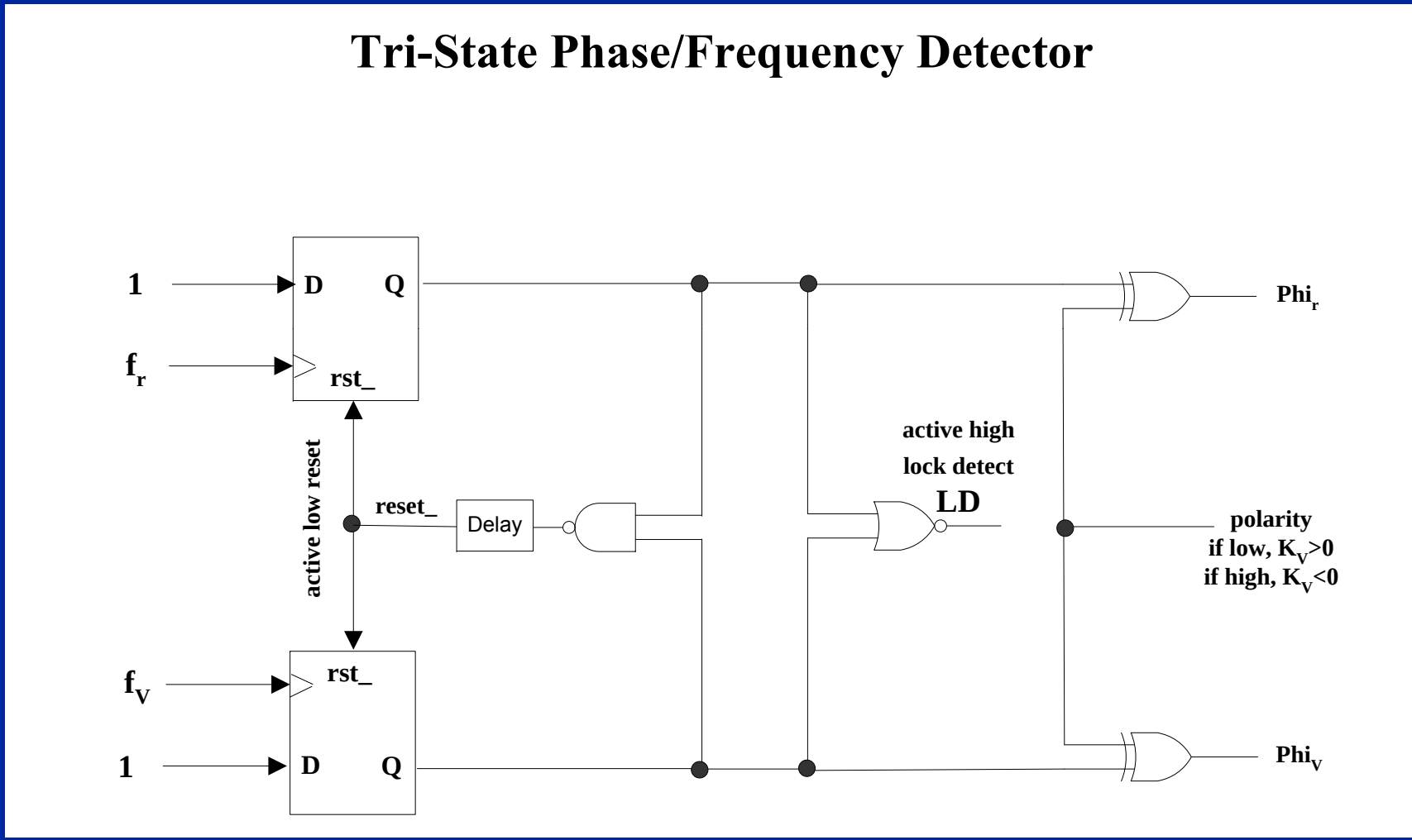
PFD Dead Zone



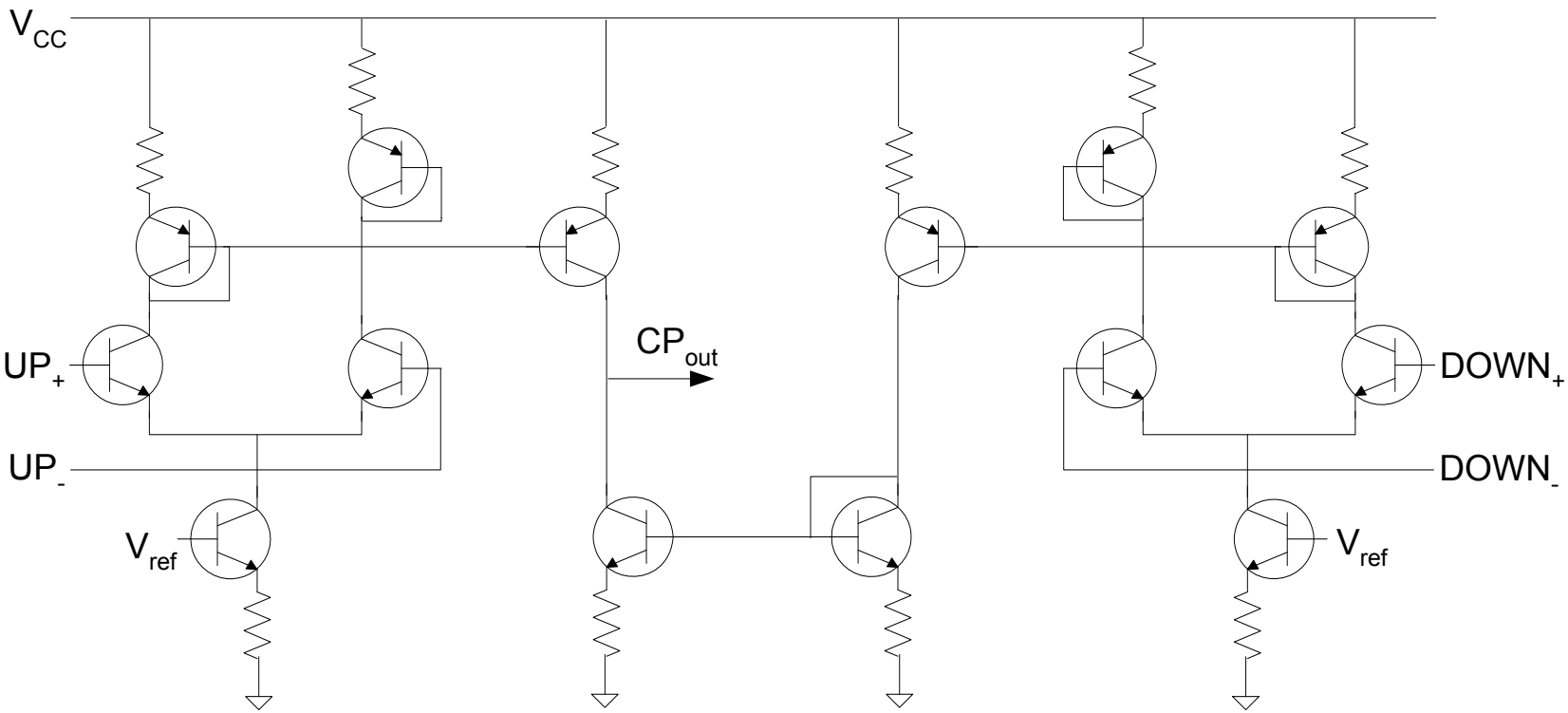




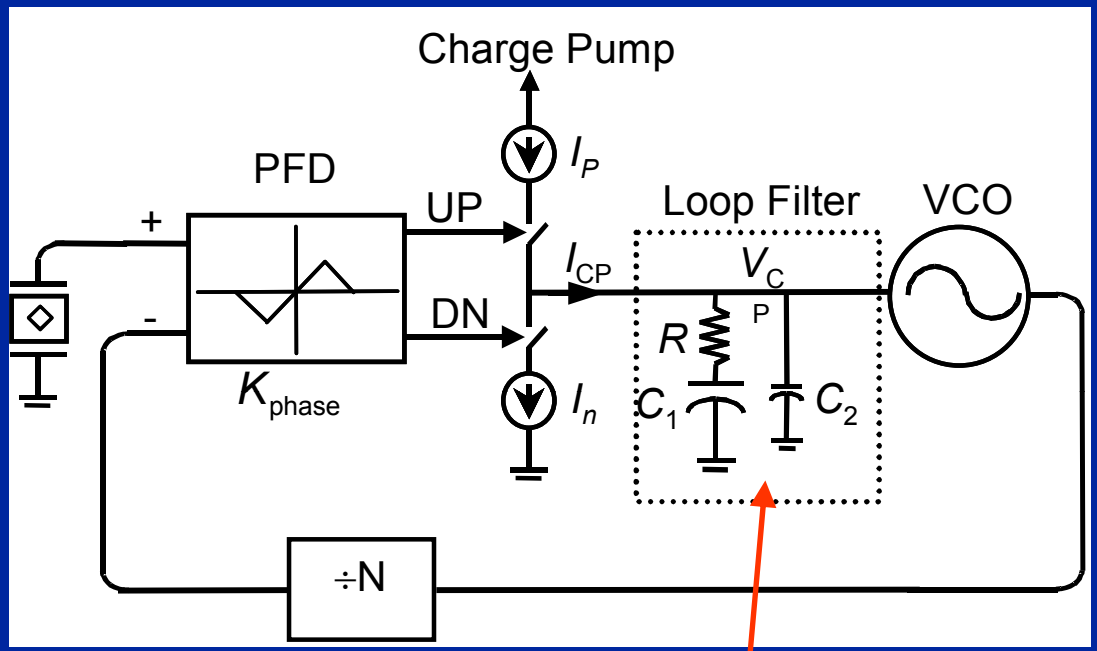
Phase/Frequency Detector



Differential Charge Pump Circuitry



2nd Order Passive Loop Filters

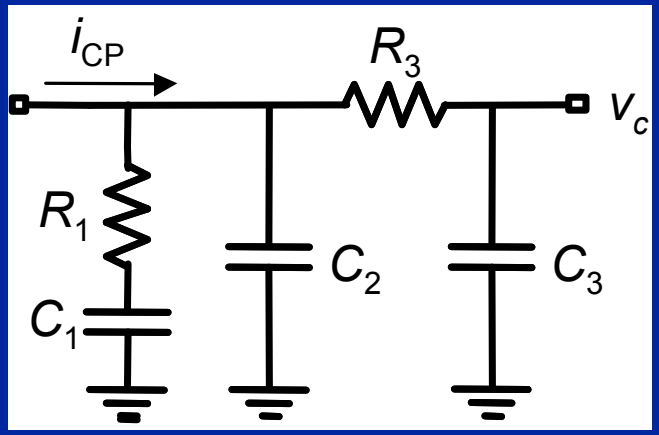


The 2nd-order filter is the highest order passive RC filter that can be built without series resistors between the charge pump and the VCO tune line

$$F(s) = \frac{(1 + sC_1R)}{s(C_1 + C_2)(1 + sC_sR)}$$

$$C_s = \frac{C_1C_2}{C_1 + C_2}$$

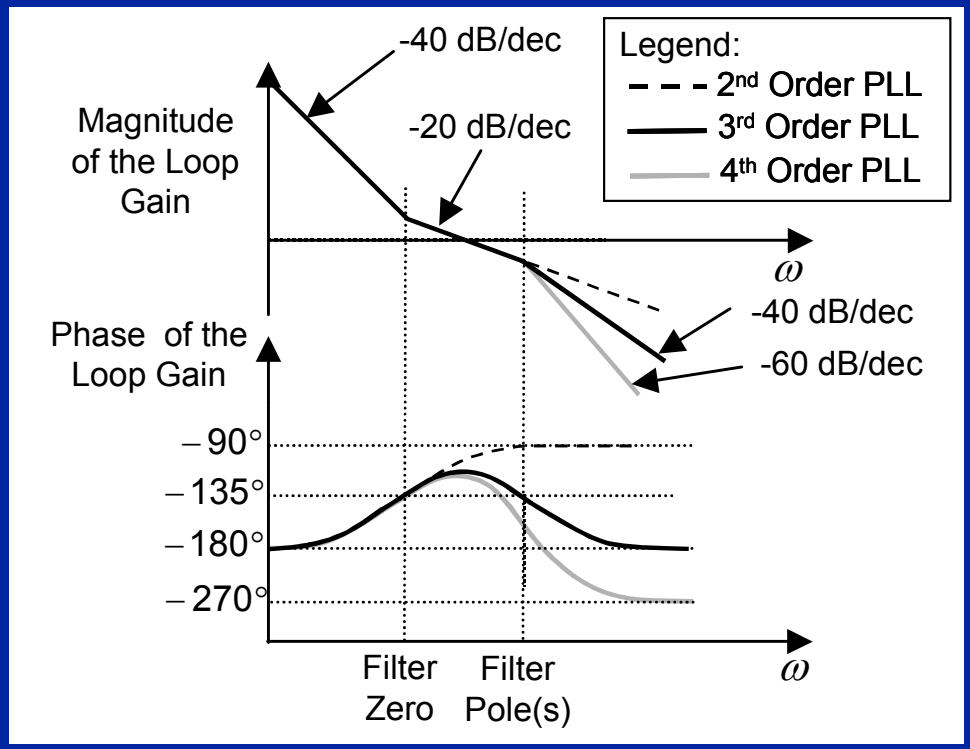
3rd Order Passive Loop Filters



$$F(s) = \frac{(1+sT_1)}{sC_t(1+sT_2)(1+sT_3)}$$

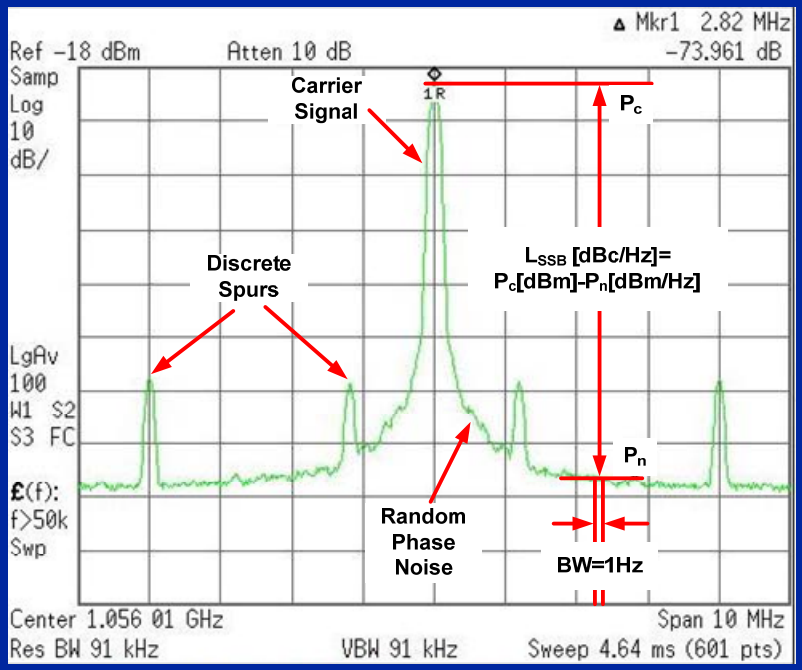
$$\begin{cases} T_1 = R_1 \cdot C_1 \\ T_2 = R_1 \cdot C_1 \cdot C_2 / C_t \\ T_3 \approx R_3 \cdot C_3 \end{cases} \qquad \begin{cases} C_i << C_1, \\ \frac{C_2}{C_3} + \frac{T_3}{T_1} >> 1 \end{cases}$$

$C_t = C1 + C2 + C3$



Comparison of open loop gain and phase in a second, third, and fourth order PLL

PLL Phase Noise and Spurs



Single sideband (SSB) phase noise power spectral density (PSD) to carrier ratio is defined as the ratio of power in one phase modulation sideband per Hertz bandwidth, at an offset $\Delta\omega$ away from the carrier, to the total signal power in units of [dBc/Hz]:

$$PN_{SSB}(\Delta\omega)=10\log\left[\frac{Noise(\omega_{LO}+\Delta\omega)}{P_{carrier}(\omega_{LO})}\right]$$

PLL output $v_{out}(t)=V_o\cos(\omega_{LO}t+\varphi_n(t))$

$\varphi_n(t)=\varphi_p\sin(\omega_m t)$

Random fluctuations in the phase

$$v_{out}(t)=V_0\cos[\omega_{LO}t+\varphi_p\sin(\omega_m t)]=$$
$$V_0[\cos(\omega_{LO}t)\cos(\varphi_p\sin(\omega_m t))-\sin(\omega_{LO}t)\sin(\varphi_p\sin(\omega_m t))]$$

For a small phase fluctuation:

$$v_0(t)=V_0[\cos(\omega_{LO}t)-\varphi_p\sin(\omega_m t)\sin(\omega_{LO}t)]$$
$$=V_0\left[\cos(\omega_{LO}t)-\frac{\varphi_p}{2}[\cos(\omega_{LO}-\omega_m)t-\cos(\omega_{LO}+\omega_m)t]\right]$$

$$PN_{SSB}(\Delta\omega)\left[\frac{dBc}{Hz}\right]=10\log\left[\frac{\frac{1}{2}\left(\frac{V_0\varphi_p}{2}\right)^2}{\frac{1}{2}V_0^2}\right]=10\log\left[\frac{\varphi_p^2}{4}\right]=10\log\left[\frac{\varphi_{rms}^2}{2}\right]$$

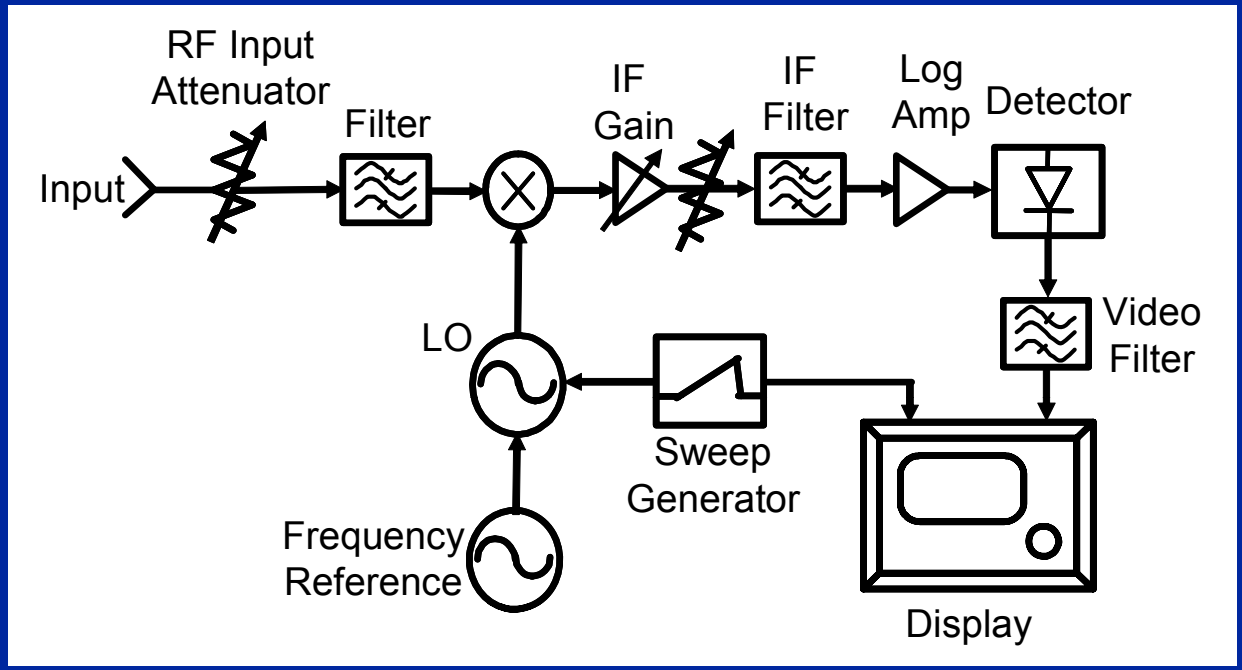
The rms phase noise or jitter:

$$\varphi_{rms}(\Delta f)=\frac{180}{\pi}\sqrt{10^{\frac{PN_{DSB}(\Delta f)}{10}}}=\frac{180\sqrt{2}}{\pi}\sqrt{10^{\frac{PN_{SSB}(\Delta f)}{10}}}\left[\text{deg}/\sqrt{\text{Hz}}\right]$$

The integrated rms phase noise or jitter:

$$\text{Jitter}_{rms}\left[rms\,\text{deg}\right]=\sqrt{\int_{\Delta f_1}^{\Delta f_2}\varphi_{rms}{}^2(f)\,df}$$

Spectrum analyzer basic block diagram

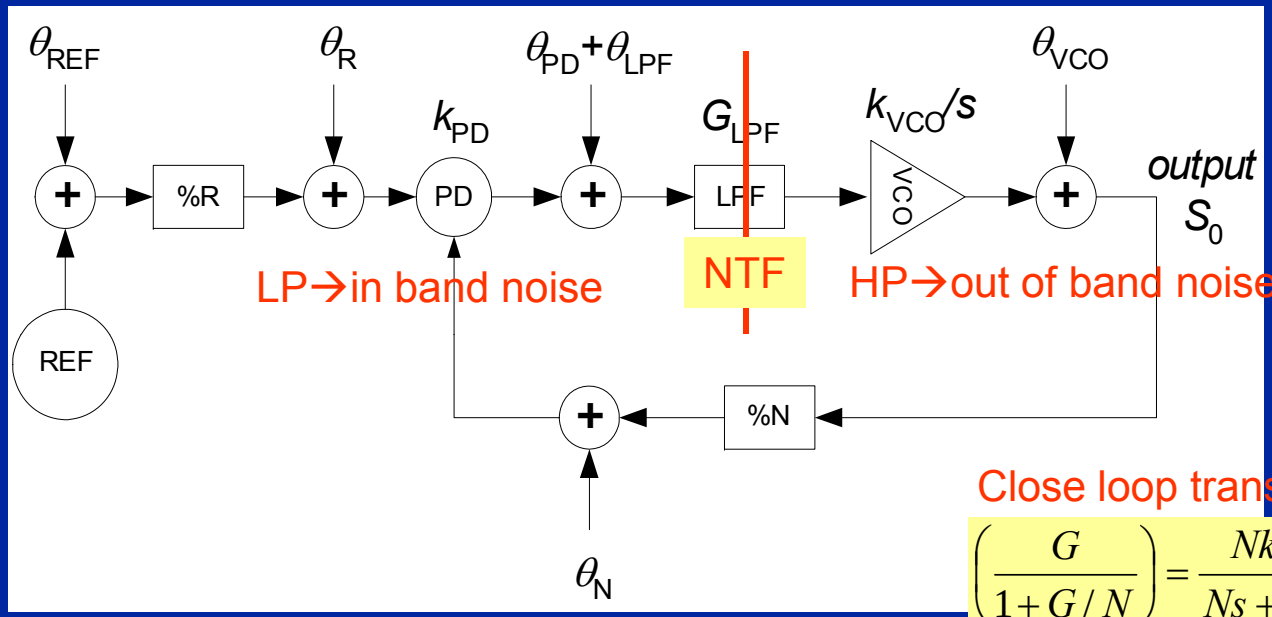


Getting the Best Sensitivity Requires Three Settings

- Narrowest resolution bandwidth
- Minimum RF attenuation
- Sufficient video filter to smooth noise (VBW < 0.01 Resolution BW)

PLL Phase Noise Sources

$$G(s) = k_{PD} G_{LPF} k_{VCO} / s$$



Close loop transfer function

$$\left(\frac{G}{1+G/N}\right) = \frac{Nk_{PD}G_{LPF}k_{VCO}}{Ns + k_{PD}G_{LPF}k_{VCO}}$$

Total output noise power spectral density

$$S_0(f) = \left[\frac{S_{REF}}{R^2} + S_R + S_N + \frac{S_{PD} + S_{LPF}}{k_{PD}^2}\right]\left(\frac{G}{1+G/N}\right)^2 + S_{VCO}\left(\frac{1}{1+G/N}\right)^2$$

LPF HPF

$$\left(\frac{1}{1+G/N}\right) = 1 - \frac{1}{N}\left(\frac{G}{1+G/N}\right)$$

In-band PLL Phase Noise

$$S_0(f)=\left[\frac{S_{REF}}{R^2}+S_R+S_N+\frac{S_{PD}+S_{LPF}}{k_{PD}^2}\right]\left(\frac{Nk_{PD}G_{LPF}k_{VCO}}{Ns+k_{PD}G_{LPF}k_{VCO}}\right)^2 \xrightarrow[s\to 0]{} \left[\frac{S_{REF}}{R^2}+S_R+S_N+\frac{S_{PD}+S_{LPF}}{k_{PD}^2}\right]N^2$$

PLL magnifies the noise from the reference, phase detector, LPF and the dividers by the amount of 20logN dB → Smaller N leads to lower in-band noise.

For integer-N Synthesizer: output frequency Fo=Fref*N, step size = Fref → cannot simultaneously achieve fine step size and small N → poor in-band noise performance.

For fractional-N Synthesizer: output frequency Fo=Fref*(N+K/F), step size = Fref/F → can achieve fine step size and small N simultaneously. → better in-band noise performance.

Out-of-Band PLL Phase Noise

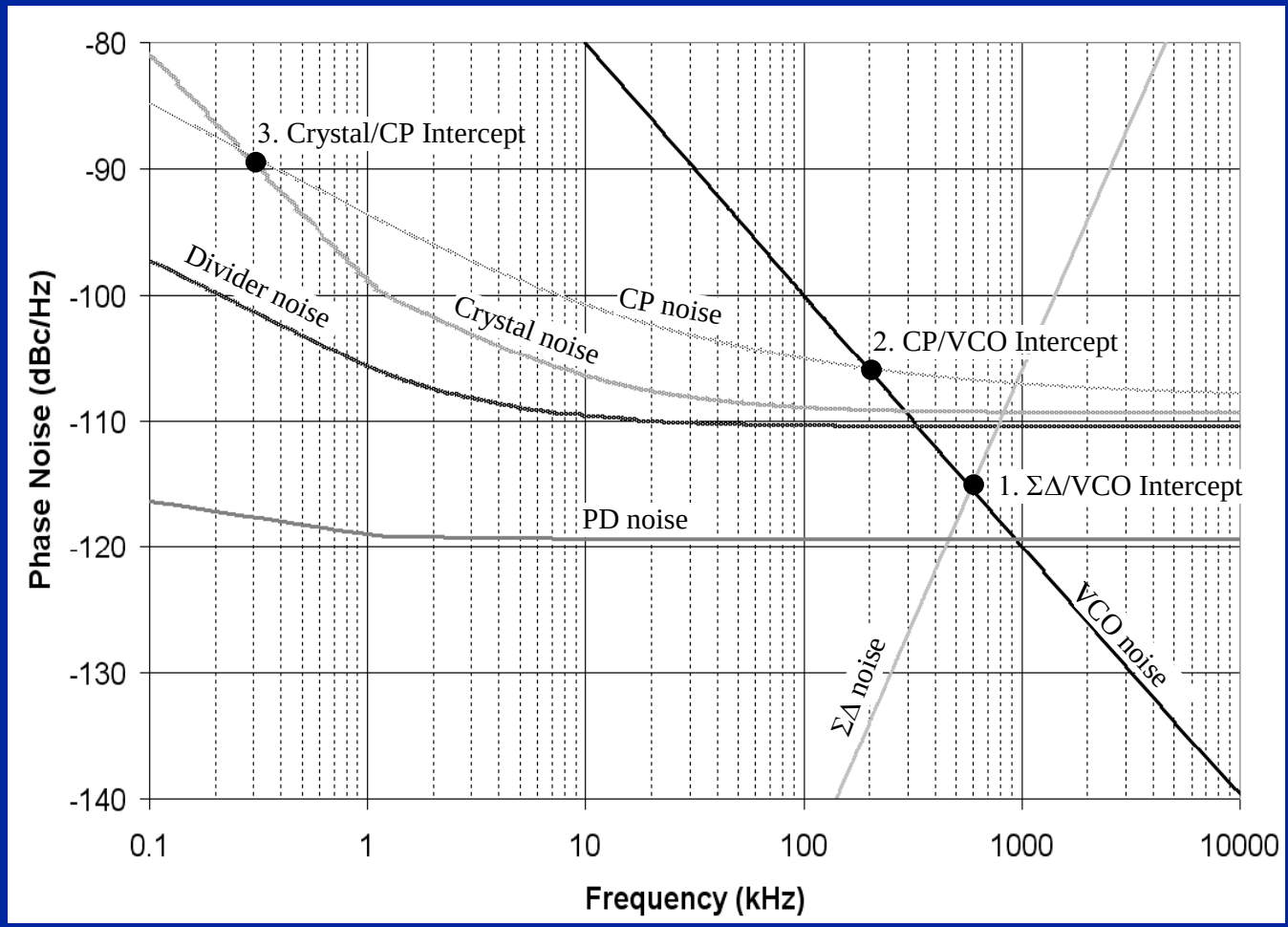
The noise outside of the PLL bandwidth is determined by the VCO phase noise, namely,

$$S_0(f) = S_{VCO}\left(\frac{1}{1+k_{PD}G_{LPF}k_{VCO}/Ns}\right)^2 \underset{s\to\infty}{\rightarrow} S_{VCO}$$

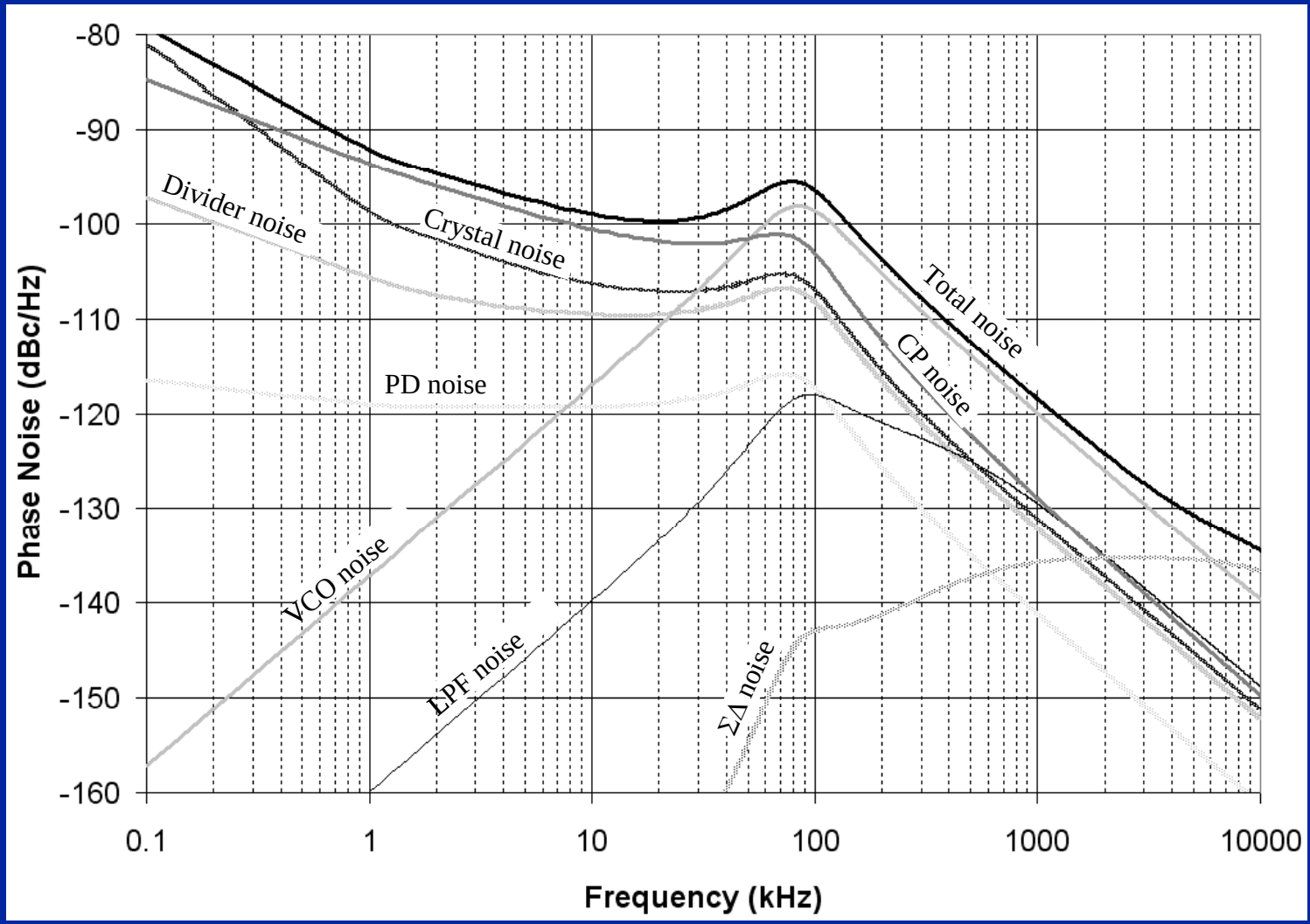
$$S_{VCO}(\Delta f) = 10\log\left\{\frac{FkT}{2P_s}\left[1+\left(\frac{f_0}{2\Delta f\cdot Q_L}\right)^2\right]\cdot\left[1+\frac{f_c}{|\Delta f|}\right]\right\}$$

Flicker 1/f noise is caused by trapping in the semiconductor material. Flicker noise corner fc is an empirical parameter depending on the device size and processing. For CMOS, fc is found to be 3~7 kHz typically and for bipolar transistors fc is about as 50 kHz. Notice that fc has impact only on close-in noise. Q_L is the loaded Q of the resonant circuit, ranging from 5~20 for on-chip resonator and 40~80 for off-chip tank. Ps is the average signal power at output of the oscillator active device, and F is oscillator effective noise factor.

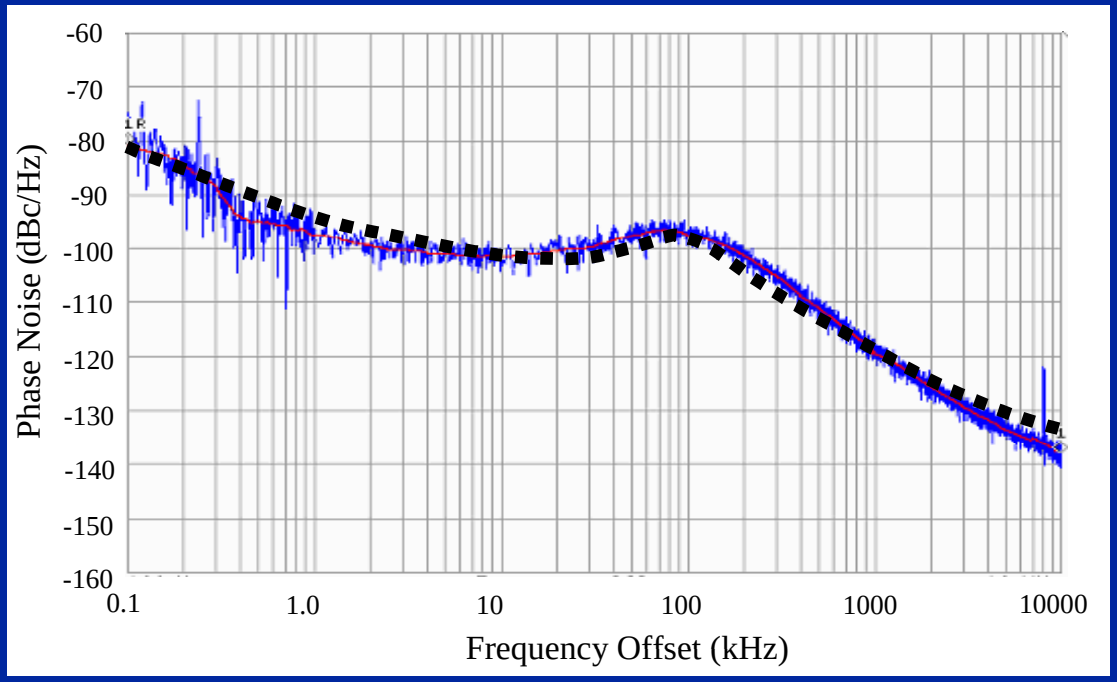
Simulated PLL Phase Noise Sources



Simulated PLL Phase Noise With Loop Effect



Comparison of Measured and Simulated Phase Noise



Frequency Band	Simulated Phase Noise	Measured Phase Noise
3.2-3.3GHz	0.44°rms	0.50°rms
4.1-4.3GHz	0.50°rms	0.535°rms

Parameter	Value
C_1	3nF
C_2	600pF
R	600Ω

References

- **J. Rogers, C. Plett, and F. Dai, "*Integrated Circuit Design for High-Speed Frequency Synthesis*," Boston: Artech House, 2006.**
- **F. Dai and C. Stroud, "Analog and Mixed-Signal Test Architectures," Chapter 15 in *System-on-Chip Test Architectures: Nanometer Design for Testability*, Morgan Kaufmann Publishers, 2007.**
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- **B. Razavi, *RF Microelectronics*, Upper Saddle River, New Jersey: Prentice Hall PTR, 1998.**
- **J. Rogers, F. F. Dai, M. S. Cavin, and D. G. Rahn, "A Fully Integrated Multi-Band SD Fractional-N Frequency Synthesizer for a MIMO WLAN Transceiver RFIC," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 3, pp. 678-689, March, 2005.**

RFIC Design and Testing for Wireless Communications

A Full-Day Tutorial at VLSI Design & Test Symposium
July 23, 2008

Lecture 3: RF Design II

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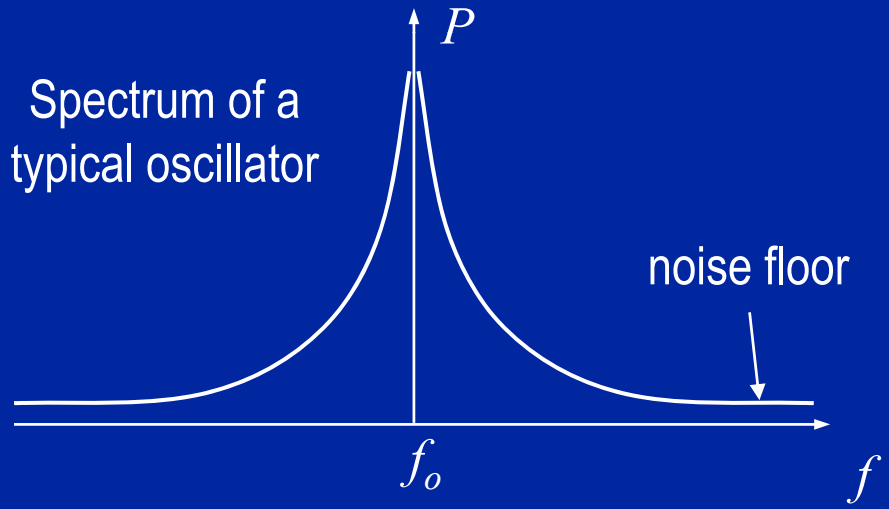
Phase Noise Specification of Oscillators

Example of oscillator periodic waveforms

- **Phase noise. We desire accurate periodicity with all signal power concentrated in one discrete oscillator frequency → an impulse function in frequency domain. However, all real oscillators have less than perfect spectral purity and thus they develop "skirts". Power in the skirts is evidence of phase noise, Phase noise is any noise that charges the frequency or phase of the oscillator waveform. Phase noise is given by:**

$$PN = P_0 / N_0$$

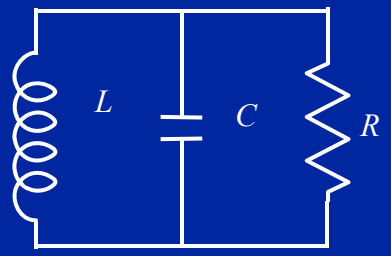


Where P_o is the power in the tone at the frequency of oscillation and N_o is the noise power spectral density at some specified offset from the carrier. Phase noise is usually specified in *dBc/Hz*, meaning noise at 1-Hz bandwidth measured in decibels with respect to the carrier.

LC Resonator – Core of Oscillators

- If $i(t) = I_{pulse}\,\delta(t)$ is applied to a parallel resonator, the time domain response of the system can be found as:

$$v_{out} = \frac{\sqrt{2} I_{pulse} e^{\frac{-t}{2RC}}}{C} \cos\left(\sqrt{\frac{1}{LC} - \frac{1}{4R^2C^2}} \bullet t\right)$$

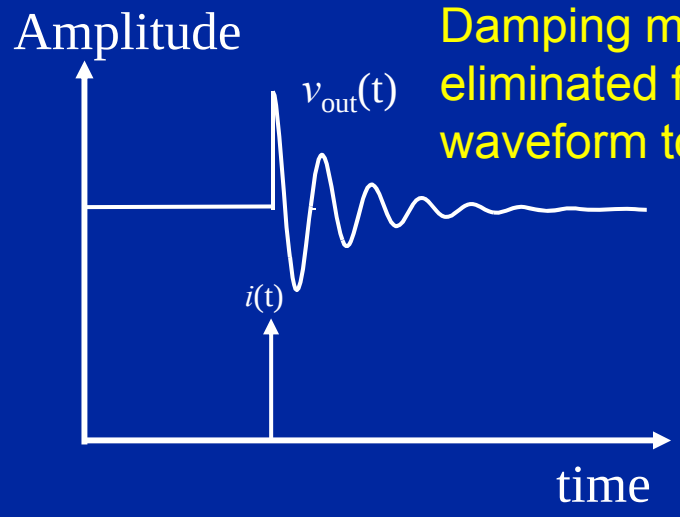


- Oscillation frequency

$$\omega_{OSC} = \sqrt{\frac{1}{LC} - \frac{1}{4R^2C^2}}$$

- In most oscillators, $|R| >> \sqrt{L/C}$

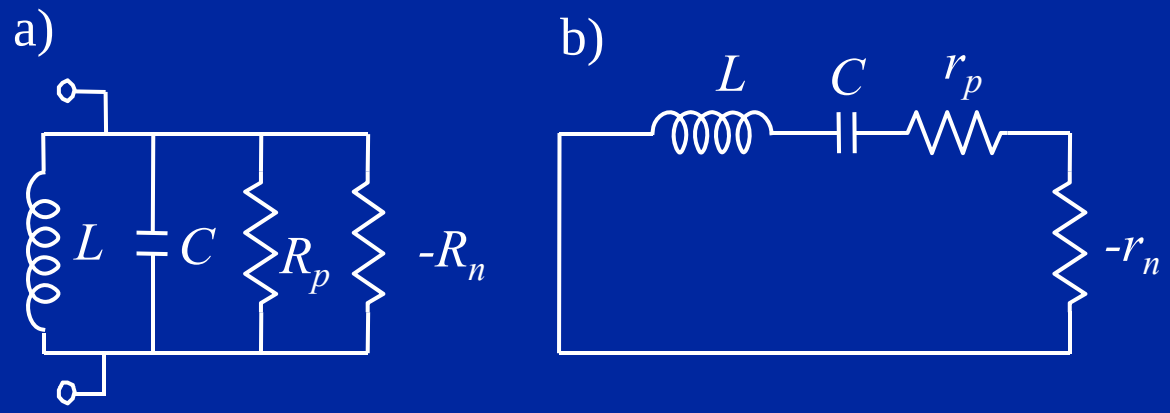
$$\omega_{OSC} = \sqrt{\frac{1}{LC}}$$



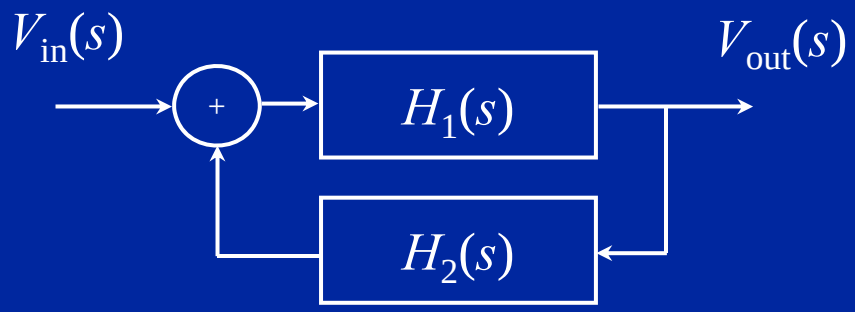
Damping must be eliminated for the waveform to persist!

Damped LC resonator with current step applied.

Adding Negative Resistance Through Feedback to Resonator



The addition of negative resistance to the circuit to overcome losses in a) a parallel resonator or b) a series resonator.



Linear model of an oscillator as a feedback control system.

Barkhausen Criterion

- Closed loop gain

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{H_1(s)}{1 - H_1(s)H_2(s)}$$

- Condition for oscillation: denominator approaches zero. → To find the closed-loop poles

$$1 - H_1(s)H_2(s) = 0$$

- For sustained oscillation at constant amplitude, the pole must be on the *jω* axis. For the open-loop analysis

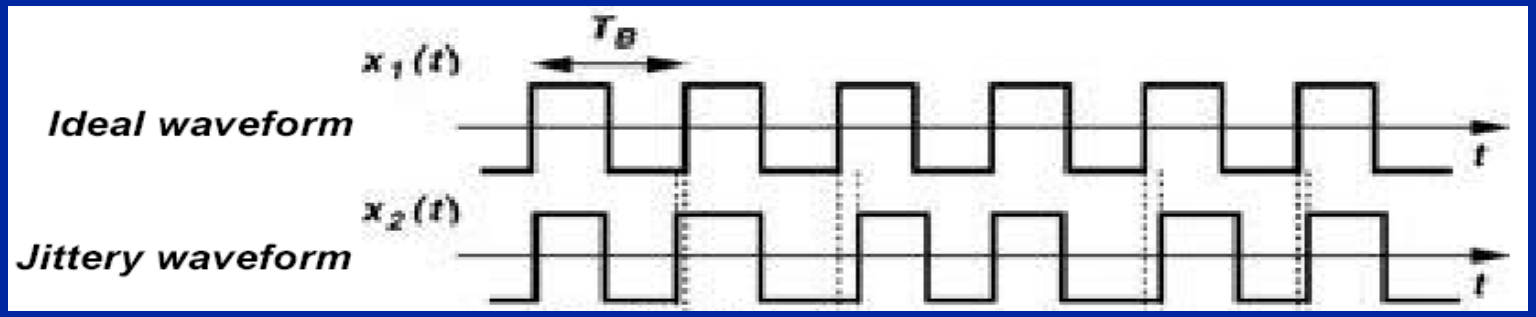
$$H_1(j\omega)H_2(j\omega) = 1$$

positive feedback with gain larger than or equal to 1.

- Barkhausen criterion, which states that for sustained oscillation at constant amplitude, the gain around the loop is 1 and the phase around the loop is 0 or some multiple of 2π.

$$\left|H_1(j\omega)\right|\left|H_2(j\omega)\right| = 1 \qquad \angle H_1(j\omega)H_2(j\omega) = 2n\pi$$

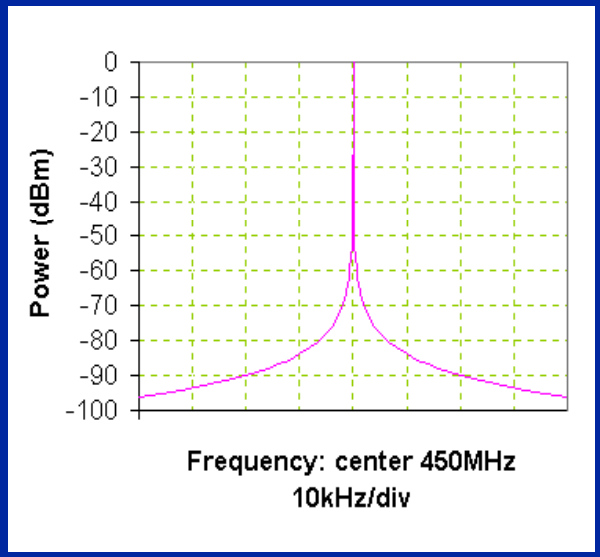
VCO Output Spectral Purity



Noise in one sideband in a 1Hz bandwidth:

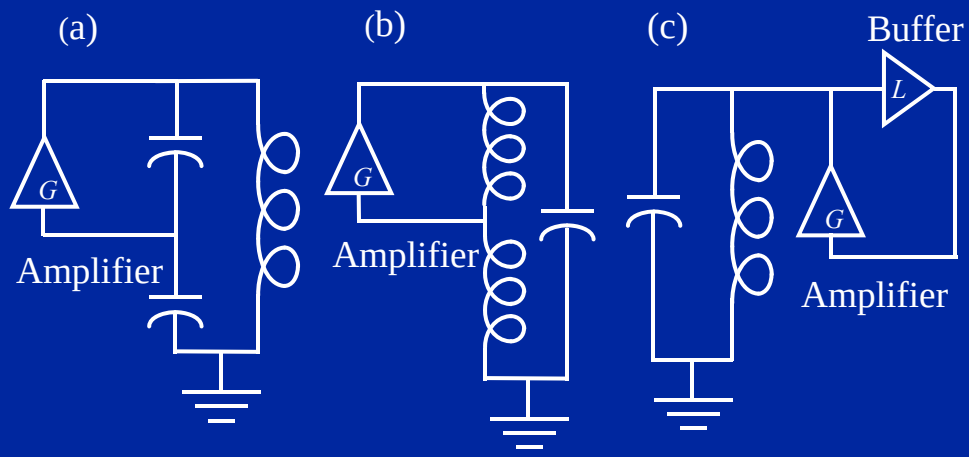
$$L_{total}(\Delta w) = \frac{\text{noise power in 1Hz BW at } w_o+\Delta w}{\text{Carrier power}}$$

Units: dBc/Hz

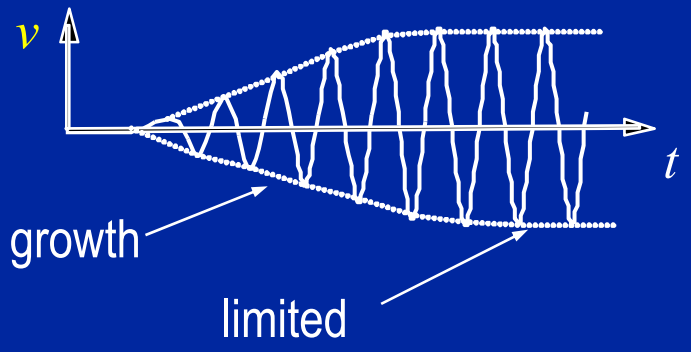


VCO Output Spectrum

Popular Implementation of Feedback to Resonator



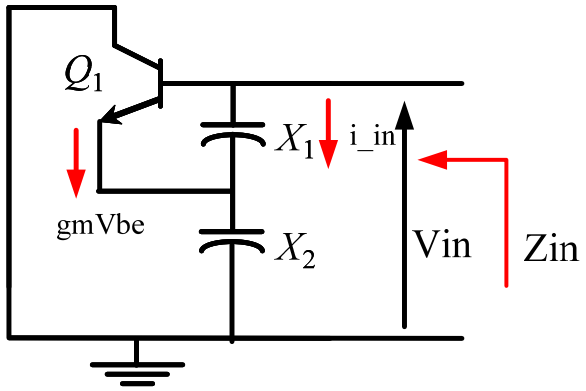
Resonators with feedback. (a) Colpitts Oscillator.
(b) Hartley Oscillator (not suitable for IC). (c) -G_m oscillator.



Waveform of an LC resonator with losses compensated. The oscillation grows until a practical constraint limits the amplitude.

Negative Resistance of Colpitts Amplifier

$$v_{in} = i_{in}\left(jX_1 + jX_2\right) + g_m v_{be}\left(jX_2\right)$$



Negative Impedance, if X_1 and X_2 are the same type

$$Z_{in} = \frac{v_{in}}{i_{in}} = -g_m X_1 X_2 + j\left(X_1 + X_2\right)$$

$$Z_{in} = -\frac{g_m}{\omega^2 C_1 C_2} + \frac{1}{j\omega C_1} + \frac{1}{j\omega C_2}$$

Load reactance needs to equal $-j(X_1+X_2)$ → add an inductor

To start the oscillation,

$$-g_m X_1 X_2 > R_L$$

$$g_m > R_L \omega^2 C_1 C_2$$

Oscillation frequency

$$f_{osc} = \frac{1}{2\pi}\left[\frac{1}{L_3}\left(\frac{1}{C_1} + \frac{1}{C_2}\right)\right]^{1/2}$$

Impedance Transform for LC Oscillator

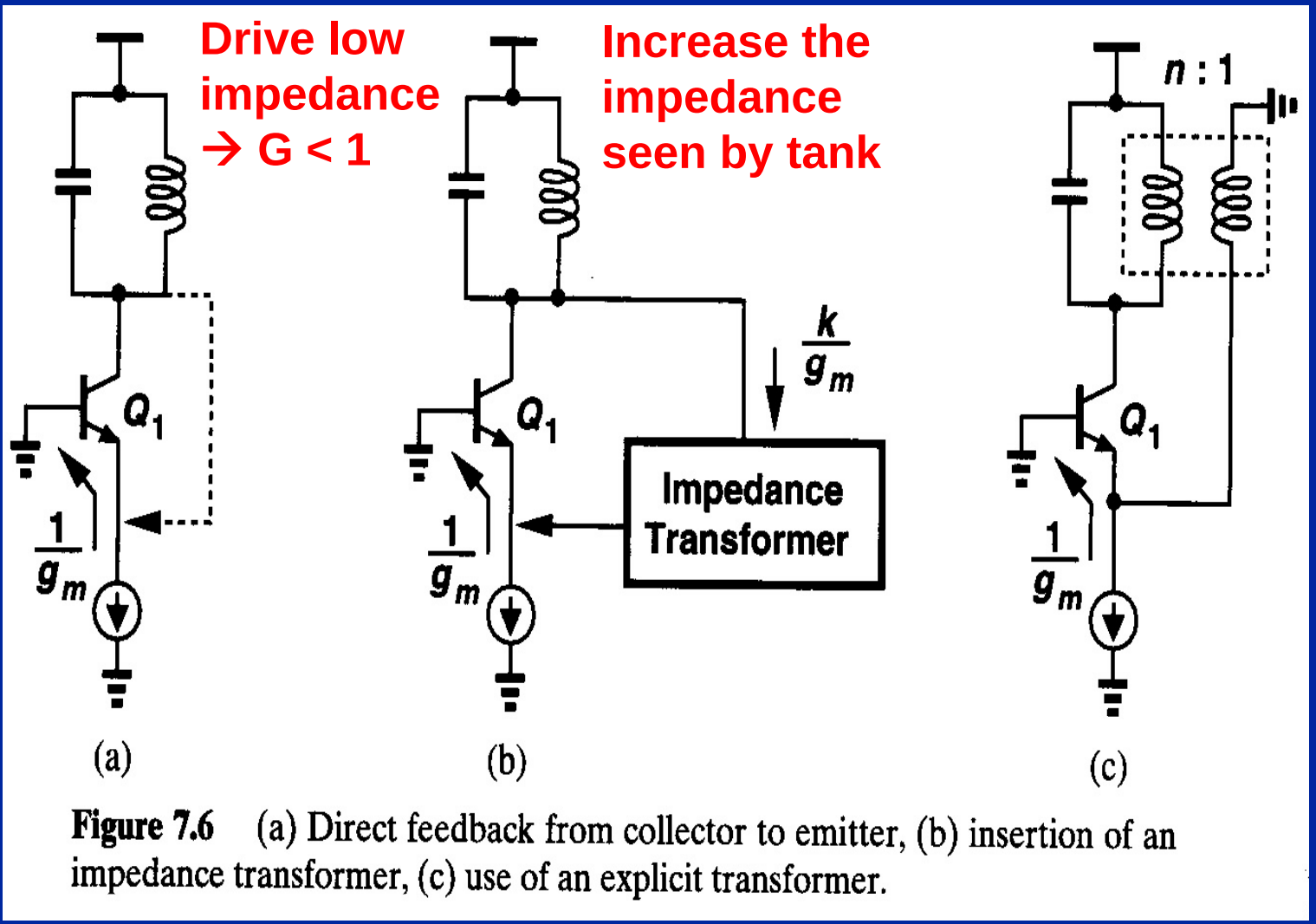
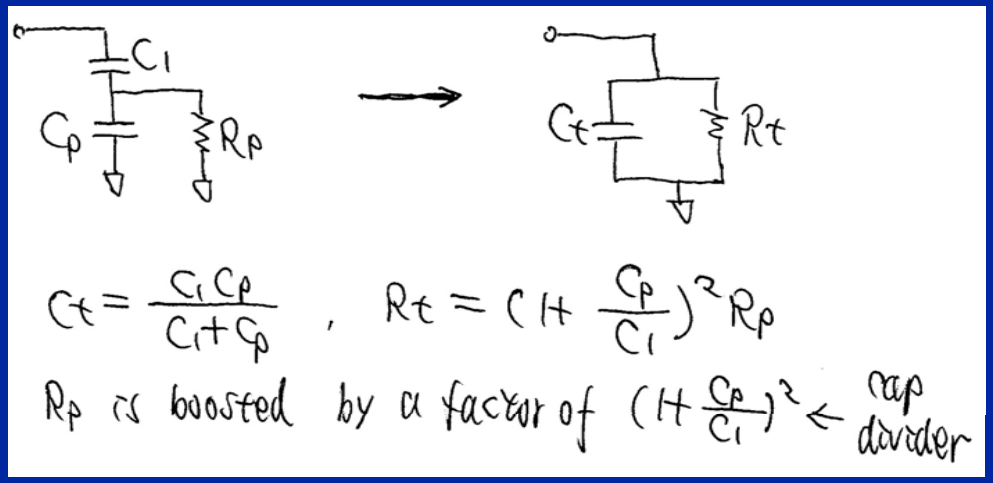


Figure 7.6 (a) Direct feedback from collector to emitter, (b) insertion of an impedance transformer, (c) use of an explicit transformer.

Passive Impedance Transformer



Impedance seen by tank =$(1+C_1/C_2)^2/g_m$

For negligible loading on the tank, $C_1 > 10C_2$ → needs a large cap.

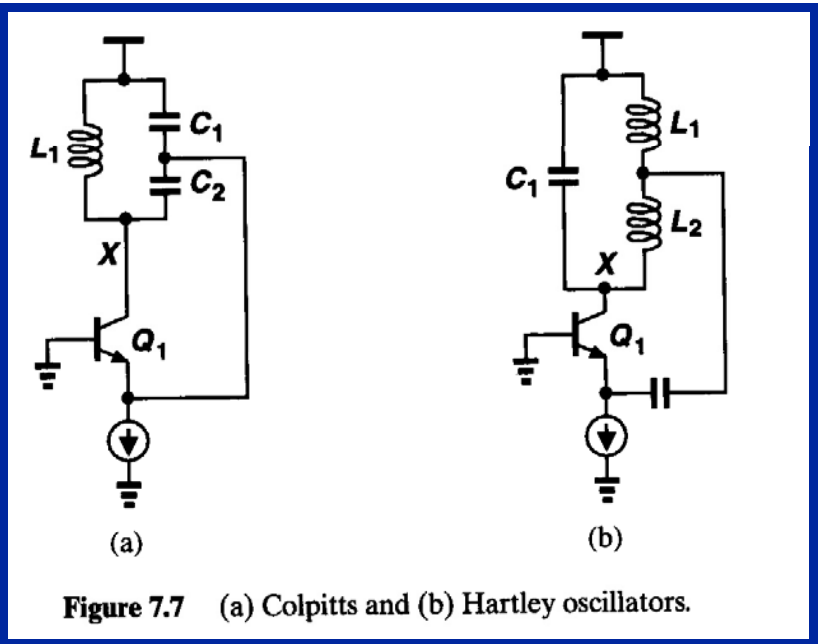
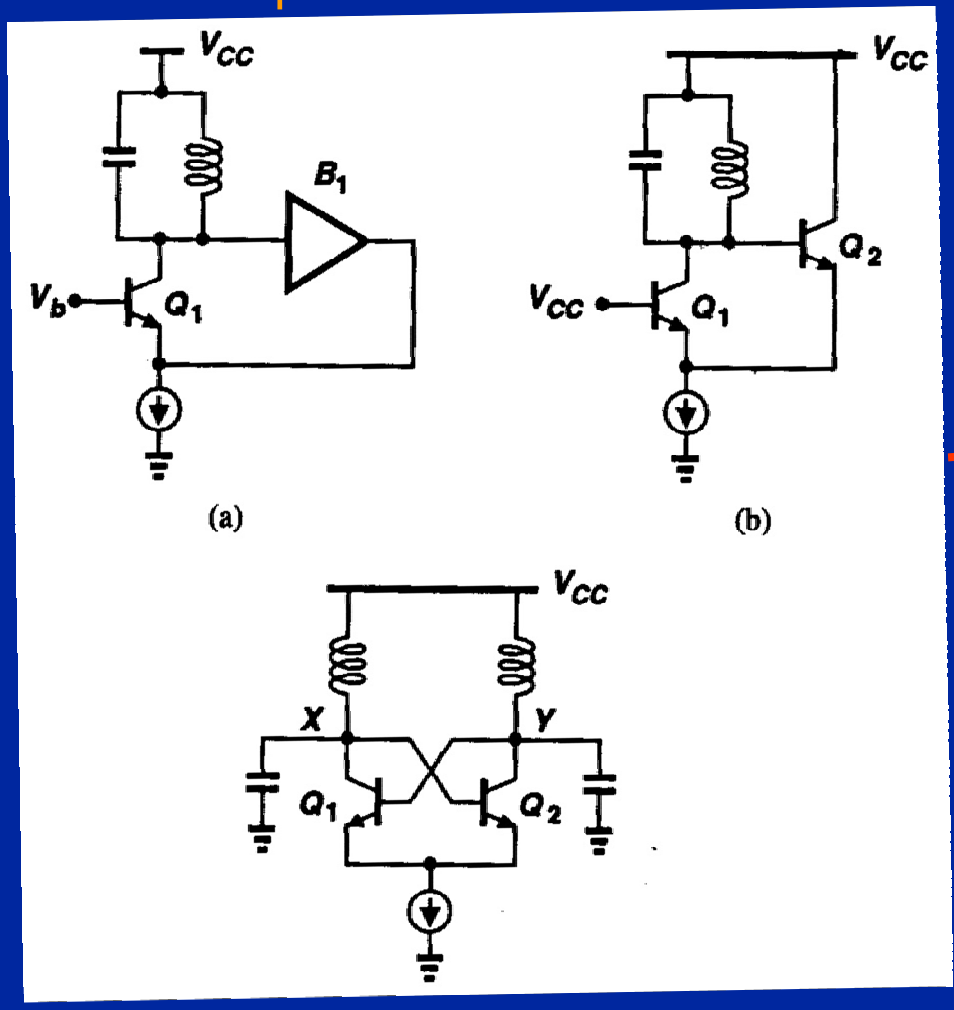


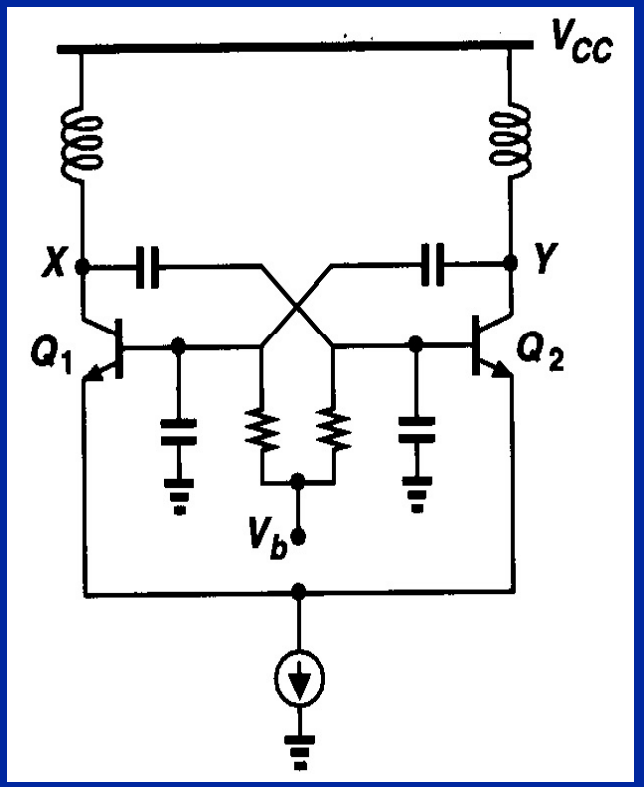
Figure 7.7 (a) Colpitts and (b) Hartley oscillators.

Impedance seen by tank = $(1+L_2/L_1)^2/g_m$

– Gm Amplifier to Cross-Coupled LC Oscillator

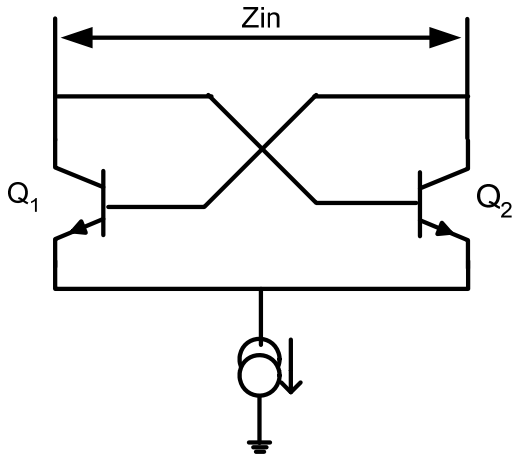
Active Impedance Transformer

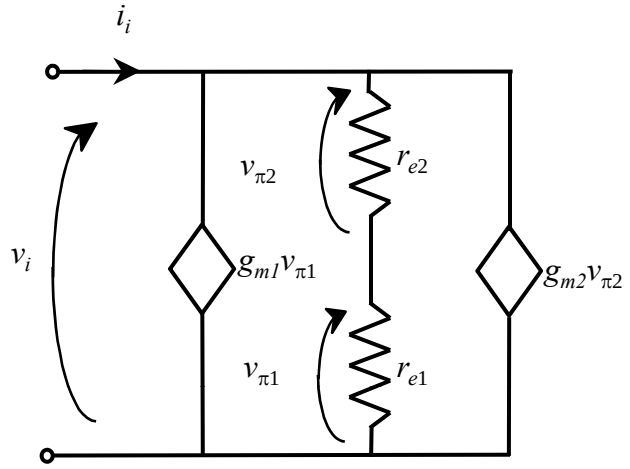




Commonly used differential VCO topology

Negative Resistance of – Gm Oscillator





$$i_i = \frac{v_i}{r_{e1} + r_{e2}} = -g_{m1}v_{\pi 1} - g_{m2}v_{\pi 2}$$

- Both transistors are biased identically,

$$Z_i = \frac{-2}{g_m}$$

- Condition for oscillation is that

$$g_m > \frac{2}{R_p}$$

where Rp is the equivalent parallel resistance of the resonator.

VCO Mathematical Model

Output frequency of an ideal VCO: $w_{out} = w_{FR} + K_{vco} V_c$

Sinusoidal output: $y(t) = A \cos \left(w_{FR} t + K_{vco} \int_{-\infty}^{t} V_c \, dt \right)$

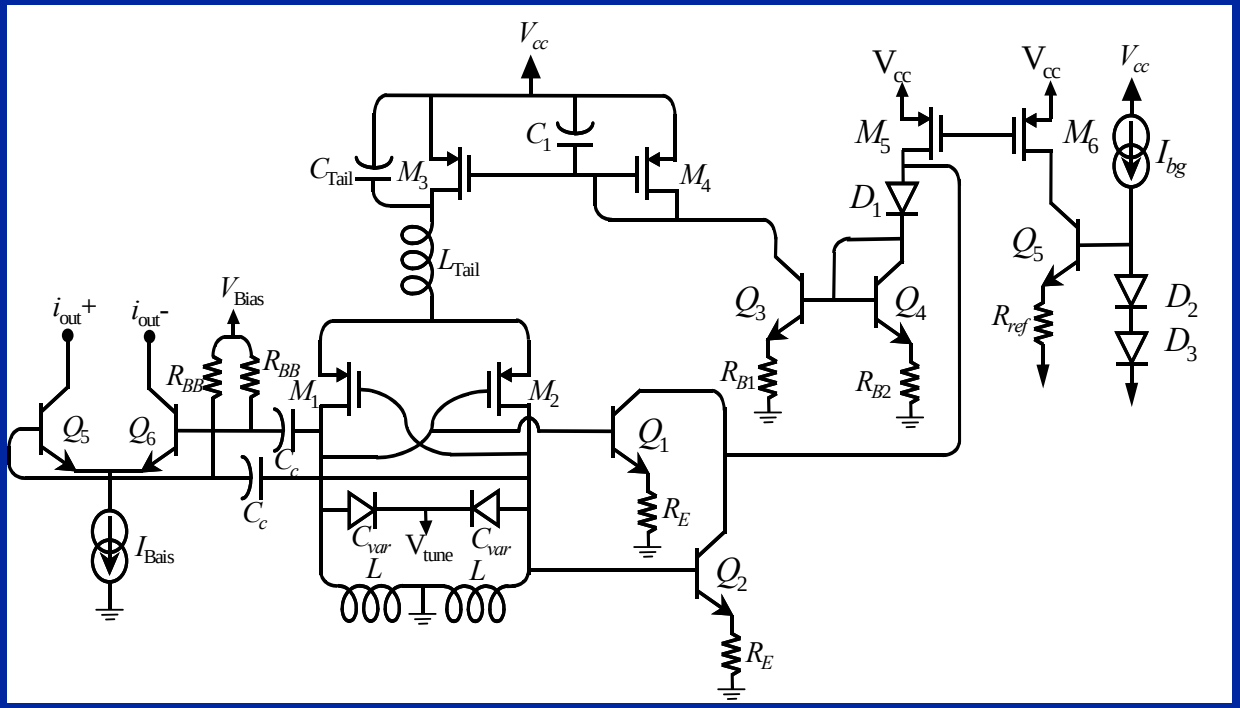
Open loop Q : $Q = (w_0/2) \left| d\varphi/dw \right|$

Where w_0 is the center frequency

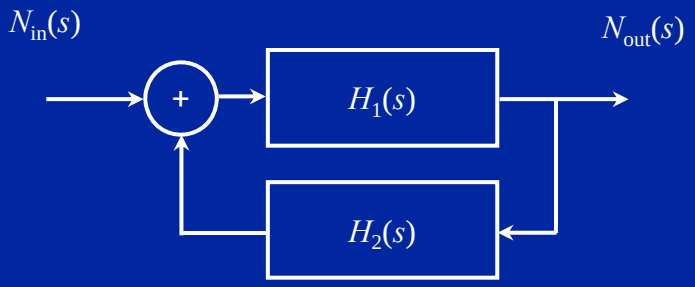
φ is the phase of open loop transfer function

PMOS VCO with Automatic Amplitude Control

- Large V_{tune} range (almost from 0V ~ Vcc V).
- Tank can be connected to ground rather than DC →lower phase noise and diodes can be connected in the proper polarity without additional biasing.
- PMOS transistors can be operated into saturation without affecting the VCO noise performance → higher output swing than bipolar VCO.
- High phase noise below 100kHz offset (due to high flicker noise) → can be tolerated by wider loop bandwidth (> 100kHz).



Linear or Additive Phase Noise - Leeson's Formula



Oscillator Phase Noise $\Phi_n(t)$

$$V_{OSC} = A\cos\left[\omega_0 t + \phi_n(t)\right]$$

- **Noise close loop transfer function**

$$\frac{N_{out}(s)}{N_{in}(s)} = \frac{H_1(s)}{1 - H(s)}$$

- Open loop transfer function
  $H(s) = H_1(s)H_2(s)$

$$H(j\omega) \approx H(j\omega_0) + \Delta\omega \frac{dH}{d\omega}$$

- Oscillation conditions

$$H(j\omega_0) = 1 \longrightarrow H_1(j\omega_0) = H_1$$

- Noise power

$$\left|\frac{N_{out}(s)}{N_{in}(s)}\right|^2 = \frac{|H_1|^2}{(\Delta\omega)^2 \left|\frac{dH}{d\omega}\right|^2}$$

Oscillator Phase Noise – Leeson's Equation

$$H(\omega) = |H| e^{j\phi}$$

$$\frac{dH}{d\omega} = \frac{d|H|}{d\omega} e^{j\phi} + |H| j e^{j\phi} \frac{d\phi}{d\omega}$$

Orthogonal

ignorable dominant

$$\left|\frac{dH}{d\omega}\right|^2 = \left|\frac{d|H|}{d\omega}\right|^2 + |H|^2 \left|\frac{d\phi}{d\omega}\right|^2$$

- **At resonance, the phase changes much faster than magnitude, and |H|=1 near resonance. → ignore amplitude noise and AM to PM conversion as well.**

$$\left|\frac{dH}{d\omega}\right|^2 = \left|\frac{d\phi}{d\omega}\right|^2 \longrightarrow \left|\frac{N_{out}(s)}{N_{in}(s)}\right|^2 = \frac{|H_1|^2}{(\Delta\omega)^2 \left|\frac{d\phi}{d\omega}\right|^2}$$

$$Q = \frac{\omega_0}{2} \left|\frac{d\phi}{d\omega}\right| \longrightarrow \left|\frac{N_{out}(s)}{N_{in}(s)}\right|^2 = \frac{|H_1|^2 \omega_0^2}{4Q^2(\Delta\omega)^2}$$

Oscillator Phase Noise – Leeson's Equation

- If feedback path is unity, then H_1=H, and since |H|=1 near resonance

$$\left|\frac{N_{out}(s)}{N_{in}(s)}\right|^2 = \frac{\omega_0^2}{4Q^2(\Delta\omega)^2}$$

- Phase noise is quoted as an absolute noise referred to the carrier power

$$PN = \frac{|N_{out}(s)|^2}{2P_S} = \left(\frac{|H_1|\omega_0}{(2Q\Delta\omega)}\right)^2 \left(\frac{|N_{in}(s)|}{2P_S}\right)$$

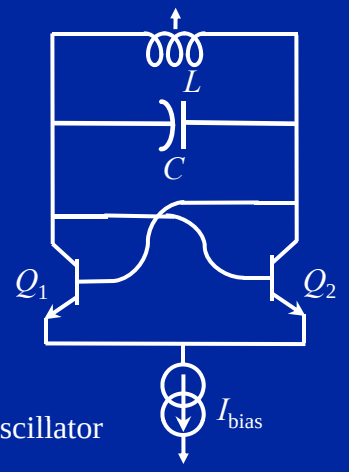
- Ps is the signal power at active device input.
- If the transistor and bias were noiseless, then the only noise present would be due to the resonator losses. The transistors and the bias will add noise to the minimum noise of

$$|N_{in}(s)|^2 = kT$$

Oscillator Phase Noise – Leeson's Equation

Active Device noise:

- If ρ is the fraction of cycle for which the transistors are completely switched, in_t is the noise current injected into the oscillator from the bias during this time.
- During transitions (1- ρ), the transistors act like an amplifier, and collector shot noise i_{cn} usually dominates.



c) -G_m Oscillator

Rp is the equivalent parallel resistance of the tank.

$$\left|N_{in}(s)\right|^2 = kT + \frac{i_{nt}^2 R_p}{2}\rho + i_{cn}^2 R_p (1-\rho)$$

Resonator loss (source)

Bias noise

Transistor shot noise

$$F = 1 + \frac{i_{nt}^2 R_p}{2kT}\rho + \frac{i_{cn}^2 R_p (1-\rho)}{kT}$$

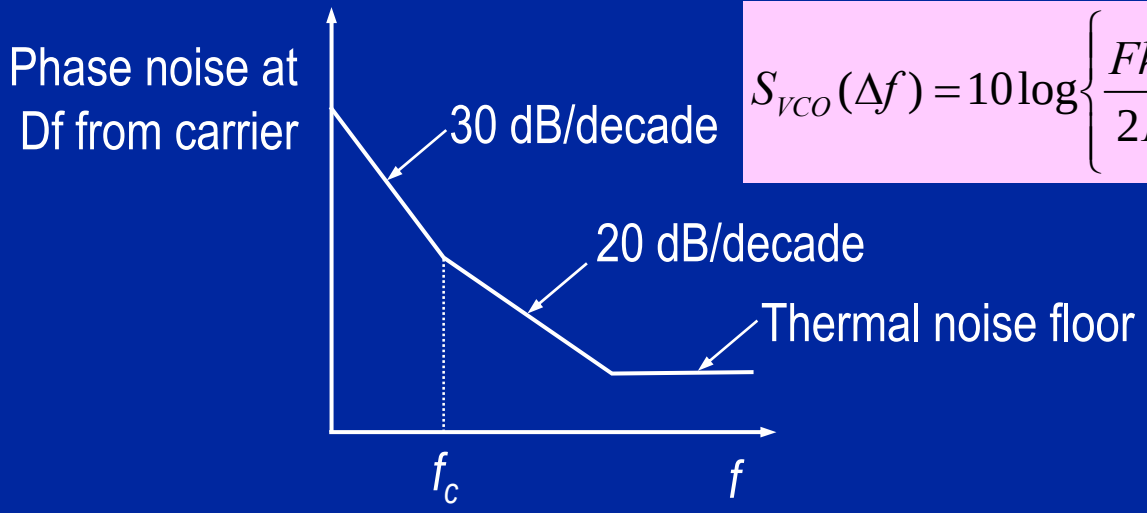
$$PN = \left(\frac{|H_1|\omega_0}{(2Q\Delta\omega)}\right)^2 \left(\frac{FkT}{2Ps}\right)$$

Oscillator Phase Noise – Leeson's Equation

- It has been assumed that flicker noise is insignificant at the frequencies of interest. This may not be the case for CMOS designs. If ω_c represents the flicker noise corner where flicker noise and thermal noise are equal,

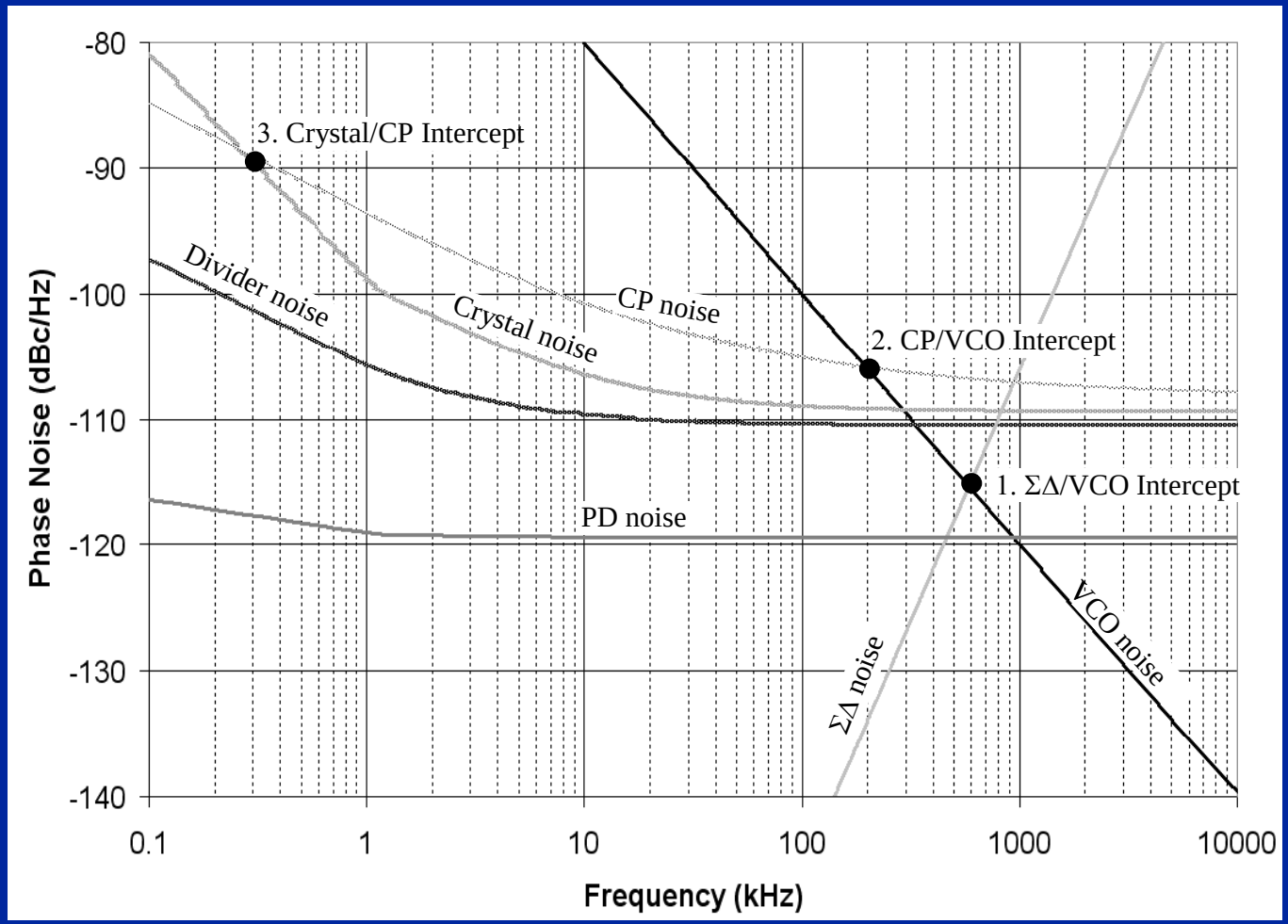
$$PN = \left(\frac{|H_1|\omega_0}{(2Q\Delta\omega)}\right)^2 \left(\frac{FkT}{2Ps}\right)\left(1+\frac{\omega_c}{\Delta\omega}\right)$$

- Assuming unity feedback, oscillator output spectrum density

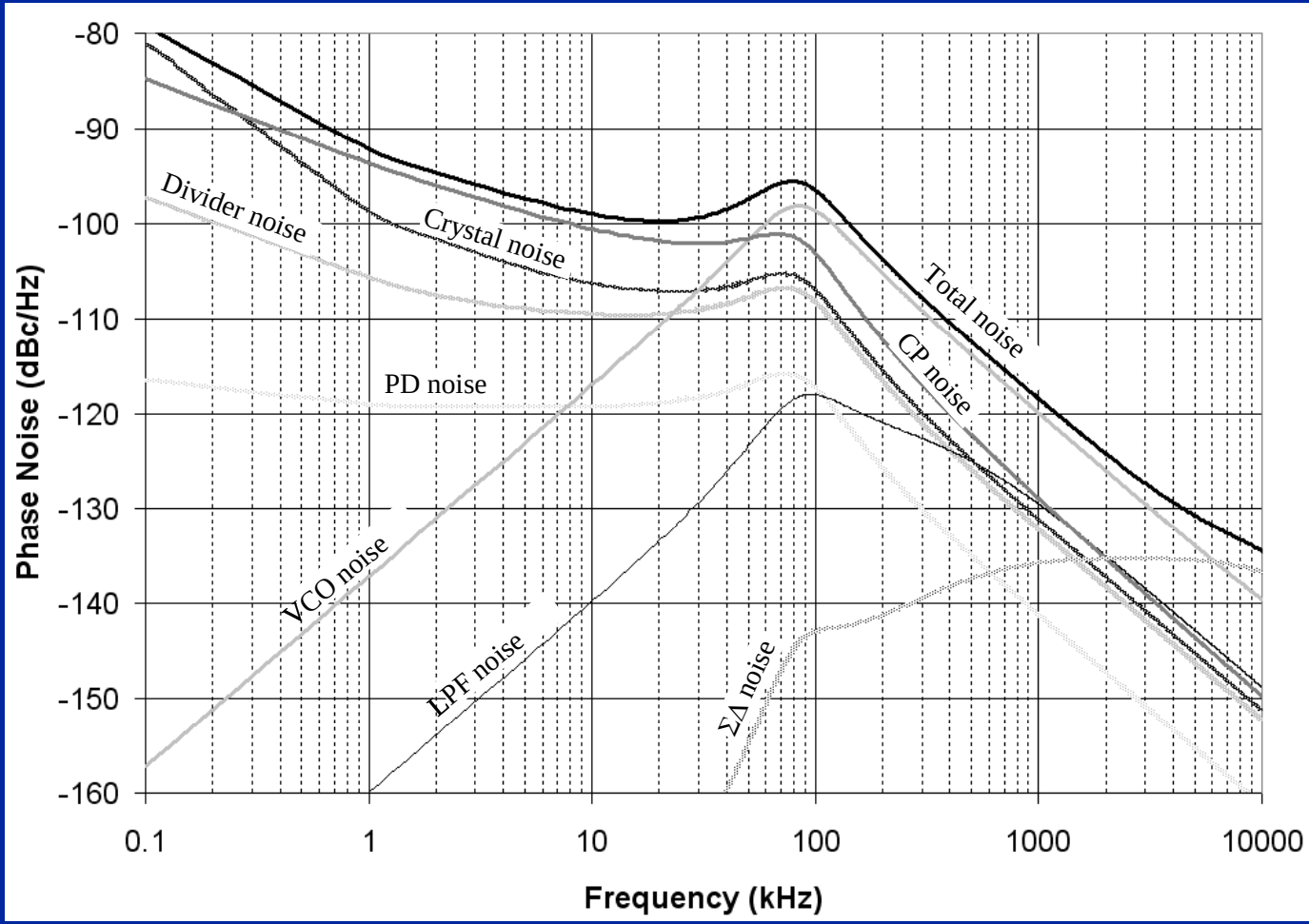


$$S_{VCO}(\Delta f) = 10\log\left\{\frac{FkT}{2P_s}\left[1+\left(\frac{f_0}{2\Delta f \cdot Q_L}\right)^2\right]\cdot\left[1+\frac{f_c}{|\Delta f|}\right]\right\}$$

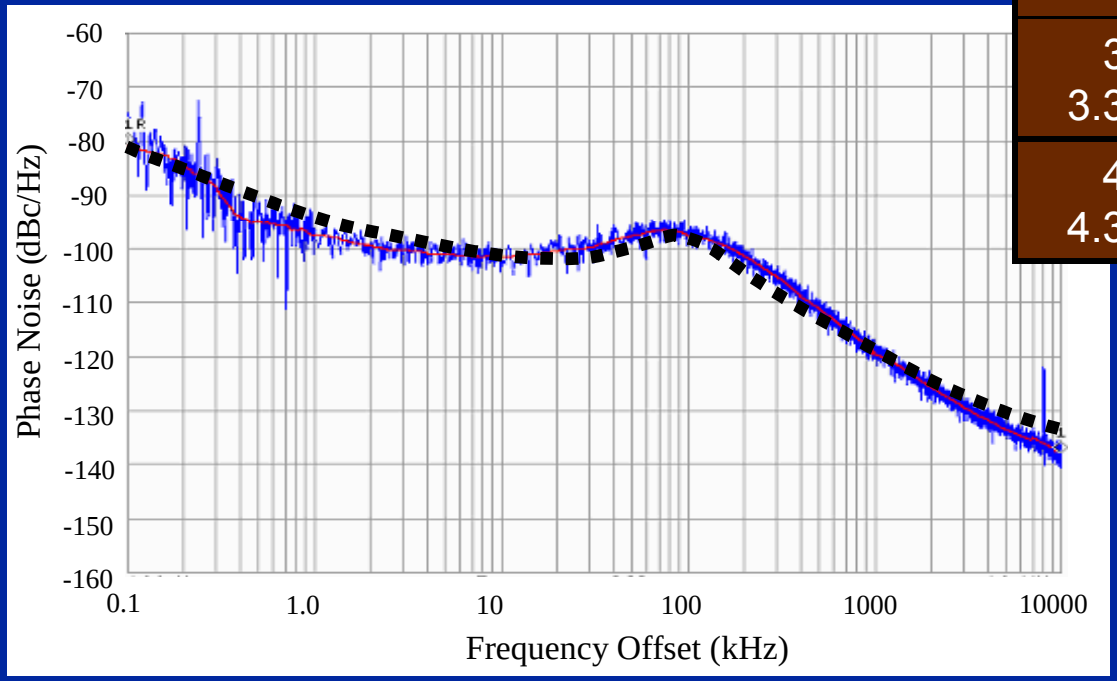
Simulated PLL Phase Noise Sources



Simulated PLL Phase Noise With Loop Effect



Comparison of Measured and Simulated Phase Noise



Frequency Band	Simulated Phase Noise	Measured Phase Noise
3.2-3.3GHz	0.44°rms	0.50°rms
4.1-4.3GHz	0.50°rms	0.535°rms

Parameter	Value
C_1	3nF
C_2	600pF
R	600Ω

RFIC Design and Testing for Wireless Communications

A Full-Day Tutorial at VLSI Design & Test Symposium
July 23, 2008

Lecture 4: Power and Gain Measurements

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Testing

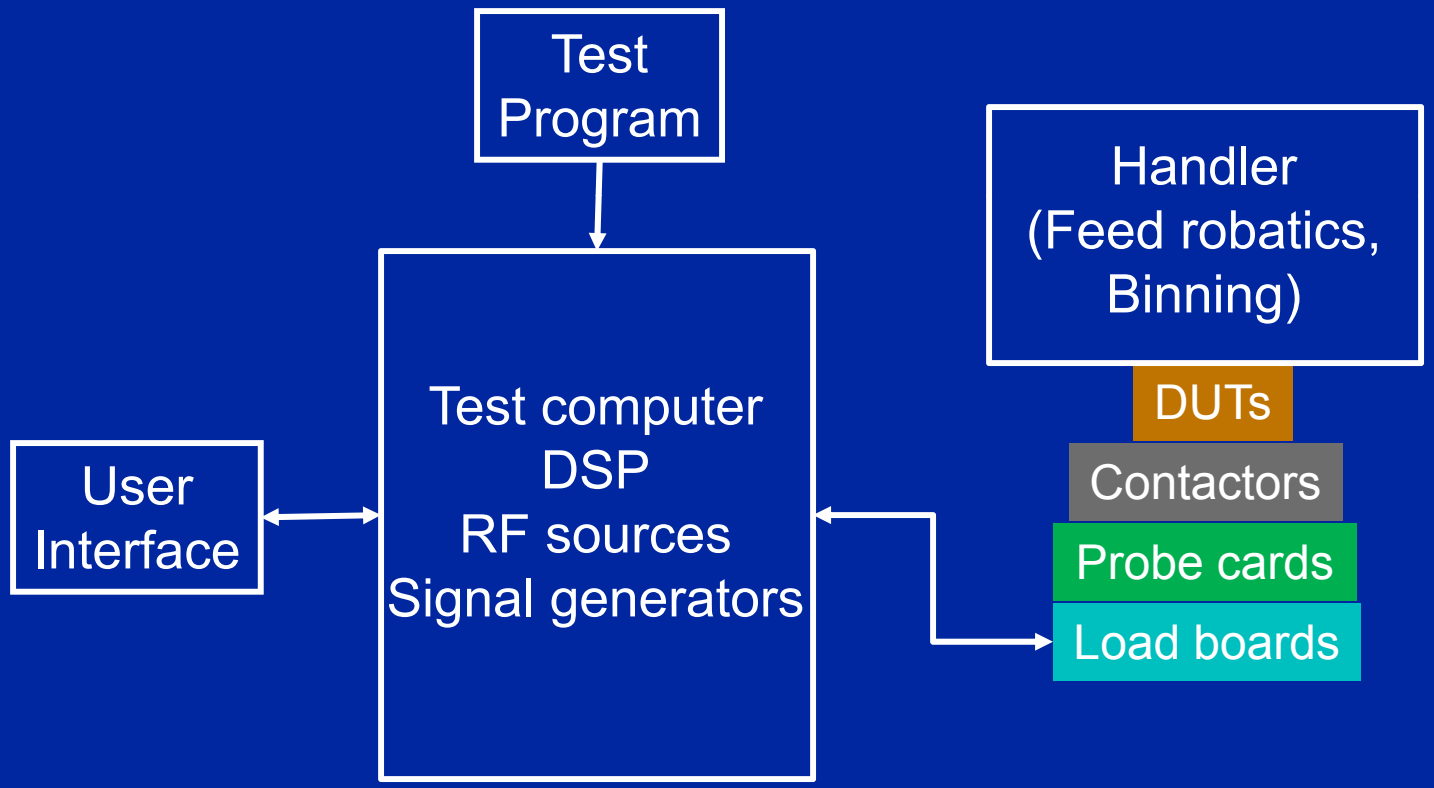
- Definition: Having designed and fabricated a device, testing must determine whether or not the device is free from any manufacturing defect.
- Testing is distinctly different from *verification*, which checks the correctness of the design.
- Forms of testing:
  - Production testing
  - Characterization testing

Production Testing

- Applied to every manufactured device
- Major considerations
  - Reduce cost; minimize test time per device.
  - Maximize quality; reduce defect level (DL), defined as fraction of bad devices passing test.
- Reference
  - M. L. Bushnell and V. D. Agrawal, *Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits*, Boston: Springer, 2000, Chapter 3.

Method of Production Testing

Automatic Test Equipment (ATE) System



Some Features of Production ATE

- Binning: Tested DUTs are grouped as
  - Passing the entire test
  - Failing any of the tests
  - Failing because of dc test
  - Failing because of RF Test
  - Failing speed (maximum clock frequency) test
- Multisite testing: Testing of several DUTs is parallelized to reduce the test cost.
- Test time for a typical device: 1 – 2 seconds.
- Testing cost of a device: 3 – 5 cents.

Characterization Testing

- Performed at the beginning of production phase.
- Objective: To verify the design, manufacturability, and test program.
- Method:
  - Few devices tested very thoroughly
  - Failures are often diagnosed
  - Tests are more elaborate than the production tests
  - Test time (and testing cost) not a consideration
  - Test program is verified and corrected in necessary
  - ATE system and additional laboratory setup may be used

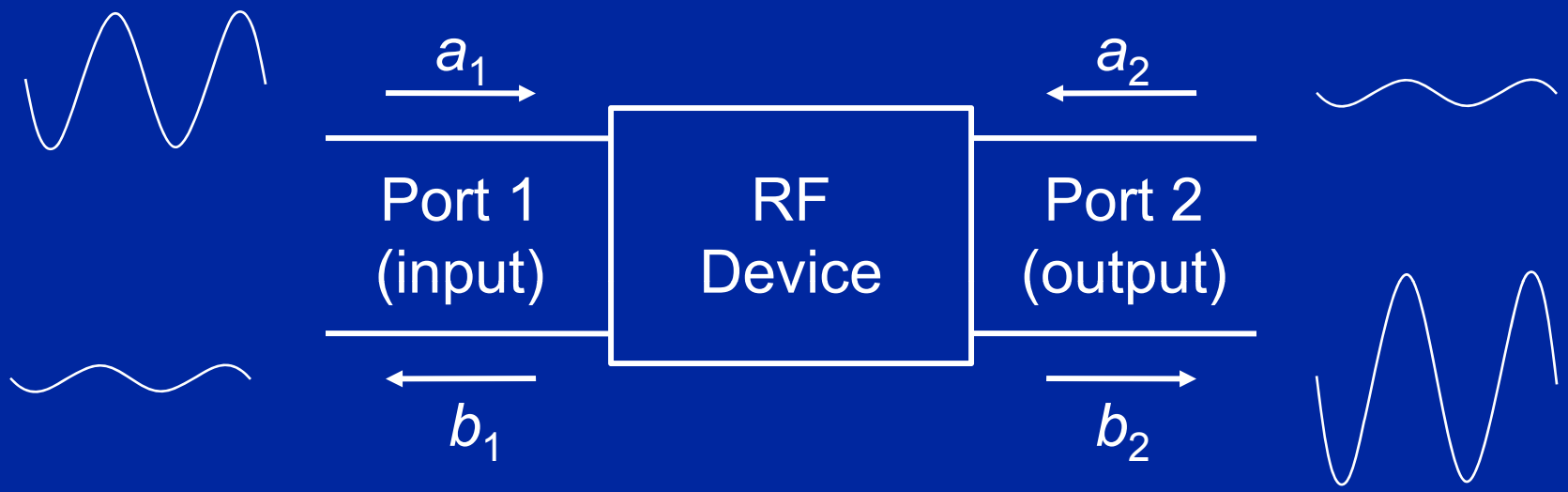
RF Tests

- Basic tests
  - Scattering parameters (S-parameters)
  - Frequency and gain measurements
  - Power measurements
  - Power efficiency measurements
- Distortion measurements
- Noise measurements

Scattering Parameters (S-Parameters)

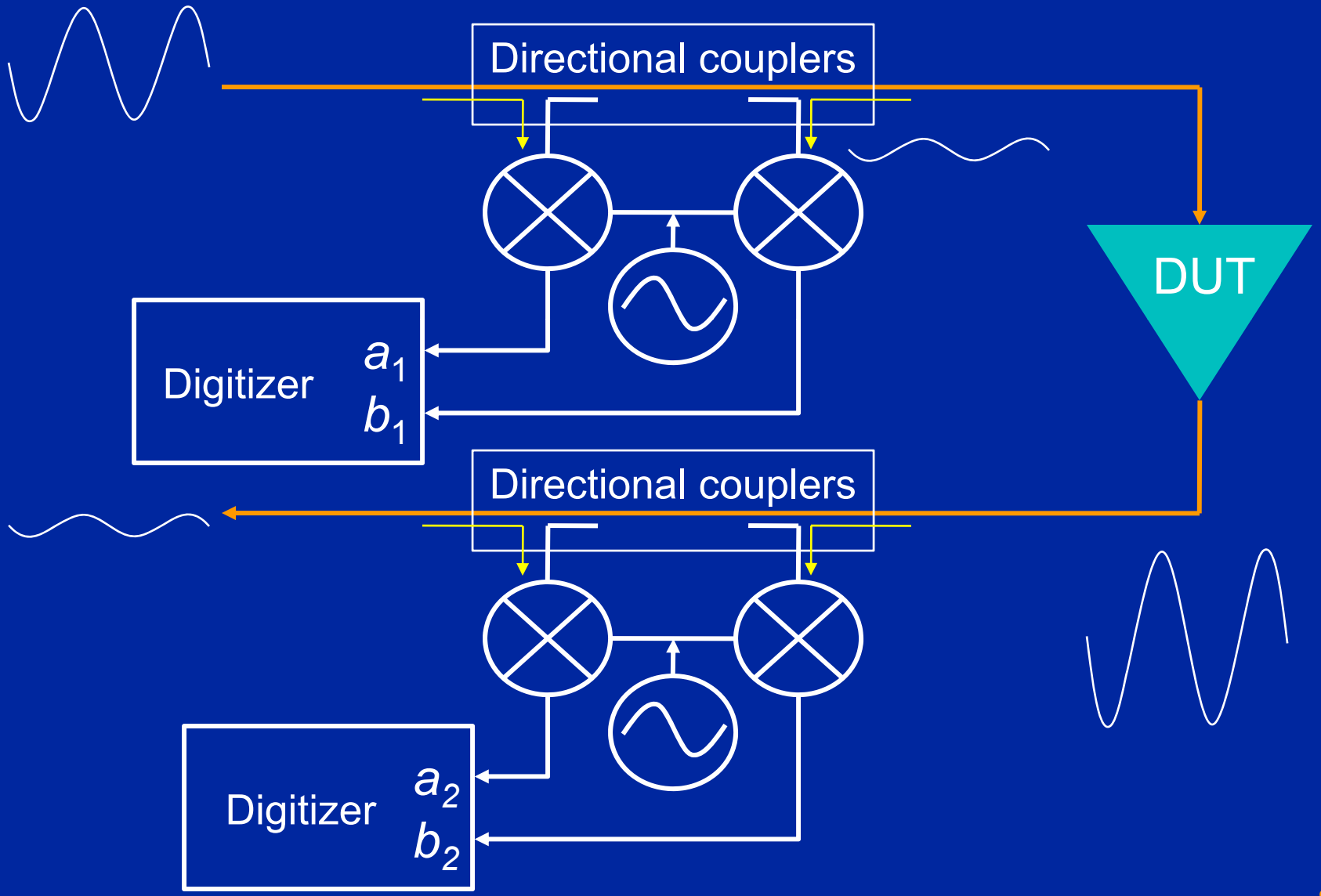
- **An RF function is a two-port device with**
  - Characteristic impedance (Z_0):
    - Z_0 = 50Ω for wireless communications devices
    - Z_0 = 75Ω for cable TV devices
  - Gain and frequency characteristics
- **S-Parameters of an RF device**
  - **S_{11} : input return loss or input reflection coefficient**
  - **S_{22} : output return loss or output reflection coefficient**
  - **S_{21} : gain or forward transmission coefficient**
  - **S_{12} : isolation or reverse transmission coefficient**
- **S-Parameters are complex numbers and can be expressed in decibels as $20 \times \log | S_{ij} |$**

Active or Passive RF Device



Input return loss	$S_{11} = b_1/a_1$
Output return loss	$S_{22} = b_2/a_2$
Gain	$S_{21} = b_2/a_1$
Isolation	$S_{12} = b_1/a_2$

S-Parameter Measurement by Network Analyzer



Application of S-Parameter: Input Match

- Example: In an S-parameter measurement setup, rms value of input voltage is 0.1V and the rms value of the reflected voltage wave is 0.02V. Assume that the output of DUT is perfectly matched. Then S_{11} determines the *input match*:
  - S_{11} = 0.02/0.1 = 0.2, or 20 × log (0.2) = –14 dB.
  - Suppose the required input match is –10 dB; this device passes the test.
- Similarly, S_{22} determines the output match.

Gain (S_{21}) and Gain Flatness

- An amplifier of a Bluetooth transmitter operates over a frequency band 2.4 – 2.5GHz. It is required to have a gain of 20dB and a gain flatness of 1dB.
- Test: Under properly matched conditions, S_{21} is measured at several frequencies in the range of operation:
  - S_{21} = 15.31 at 2.400GHz
  - S_{21} = 14.57 at 2.499GHz
- From the measurements:
  - At 2.400GHz, Gain = 20×log 15.31 = 23.70 dB
  - At 2.499GHz, Gain = 20×log 14.57 = 23.27 dB
- Result: Gain and gain flatness meet specification. *Measurements at more frequencies in the range may be useful.*

Power Measurements

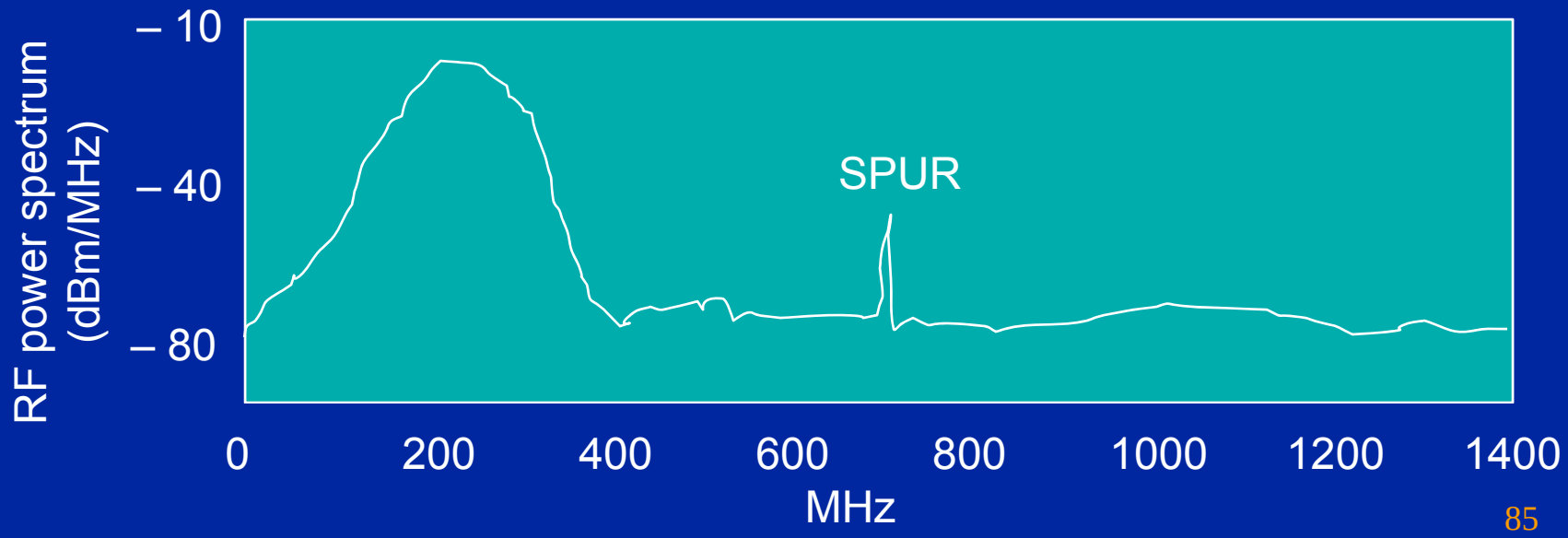
- Receiver
  - Minimum detectable RF power
  - Maximum allowed input power
  - Power levels of interfering tones
- Transmitter
  - Maximum RF power output
  - Changes in RF power when automatic gain control is used
  - RF power distribution over a frequency band
  - Power-added efficiency (PAE)
- Power unit: dBm, relative to 1mW
  - Power in dBm = 10 × log (power in watts/0.001 watts)
  - Example: 1 W is 10×log 1000 = 30 dBm
  - What is 2 W in dBm?

Power Spectrum Measurements

- Spur measurement
- Harmonic measurement
- Adjacent channel interference

Spur Measurement

- "Spur" is a spurious or unintended frequency in the output of an RF device.
- Example: leakage of reference frequency used in the phase detector of PLL.
- A spur can violate the channel interference standard of a communication system.
- Complete power spectrum measured in characterizing phase to determine which interfering frequencies should be checked during production testing.



Harmonic Measurements

- Multiples of the carrier frequency are called harmonics.
- Harmonics are generated due to nonlinearity in semiconductor devices and clipping (saturation) in amplifiers.
- Harmonics may interfere with other signals and must be measured to verify that a manufactured device meets the specification.

Adjacent Channel Power Ratio (ACPR)

- Ratio of average power in the adjacent frequency channel to the average power in the transmitted frequency channel.
- Also known as adjacent channel leakage ratio (ACLR).
- A measure of transmitter performance.

Power-Added Efficiency (PAE)

- Definition: Power-added efficiency of an RF amplifier is the ratio of RF power generated by the amplifier to the DC power supplied:
  - $PAE = \Delta P_{RF} / P_{DC}$ where
    - $\Delta P_{RF} = P_{RF}(output) - P_{RF}(input)$
    - $P_{dc} = V_{supply} \times I_{supply}$
- Important for power amplifier (PA).
- 1 – PAE is a measure of heat generated in the amplifier, i.e., the battery power that is wasted.
- In mobile phones PA consumes most of the power. A low PAE reduces the usable time before battery recharge.

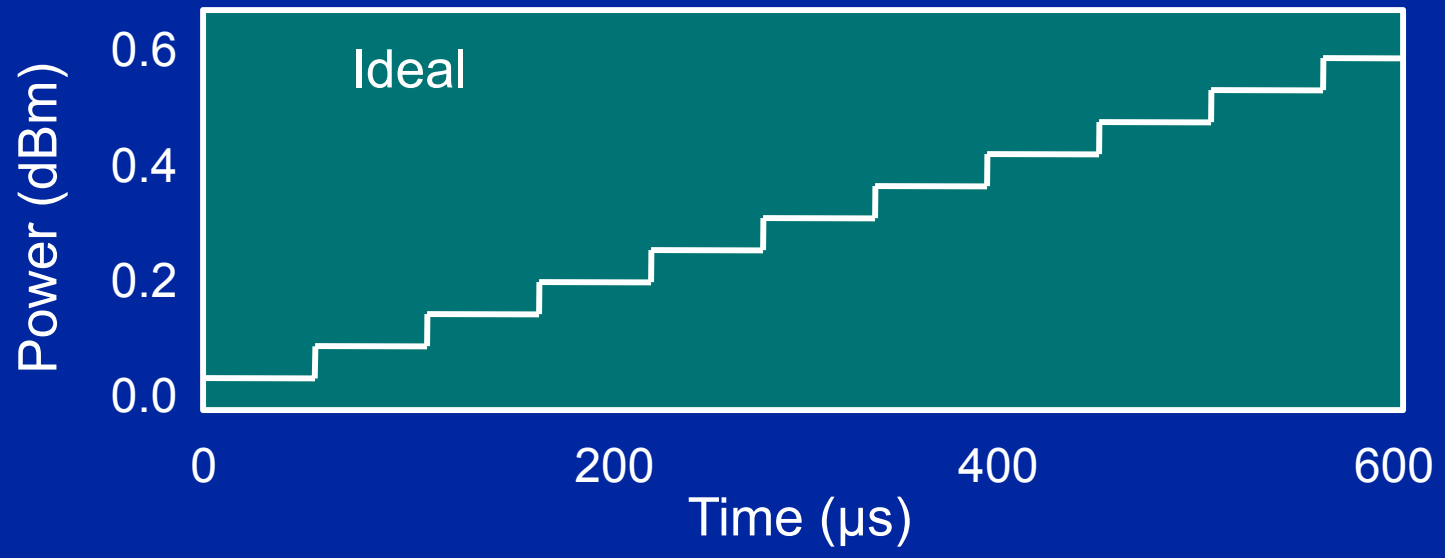
PAE Example

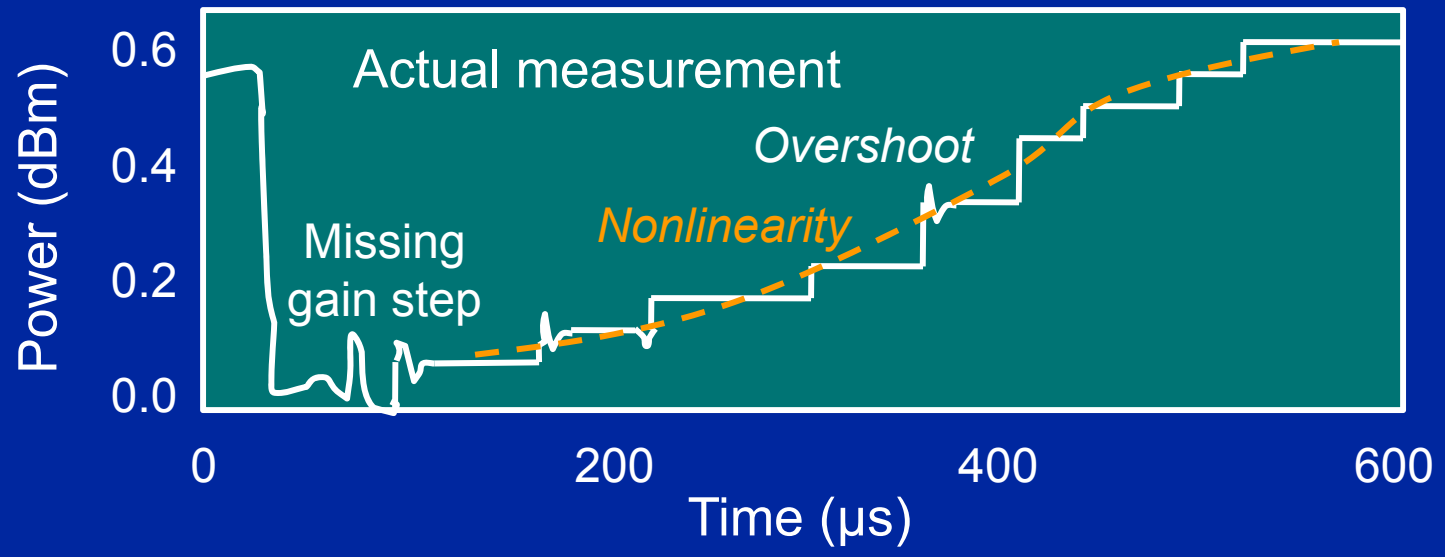
- Following measurements are obtained for an RF power amplifier:
  - RF Input power = +2dBm
  - RF output power = +34dBm
  - DC supply voltage = 3V
  - DUT current = 2.25A
- PAE is calculated as follows:
  - $P_{RF}(input) = 0.001 \times 10^{2/10} = 0.0015W$
  - $P_{RF}(output) = 0.001 \times 10^{34/10} = 2.5118W$
  - $P_{dc} = 3 \times 2.25 = 6.75W$
  - PAE = (2.5118 – 0.00158)/6.75 = 0.373 or 37.2%

Automatic Gain Control Flatness(SOC DUT)

- Tester pseudocode:
  - Set up input signal to appropriate frequency and power level
  - Set up output measurement equipment to receive output signal when triggered
  - Program SOC AGC to first gain level and trigger receiver
    - Cycle SOC AGC to next gain level
    - Wait long enough to capture relevant data
    - Cycle to next gain level and repeat though all levels
- Transfer time-domain data to host computer for processing
  - Power at ith gain level = $20 \times \log [V_R(i)^2 + V_i(i)^2]^{1/2} + 13$ dBm for 50Ω characteristic impedance, where V_R and V_i are the measured real and imaginary voltages

AGC – Other Characteristics





AGC Characteristics to be Verified

- Gain errors and missing levels
- Overshoots and undershoots – settling time
- Finite (non-zero) transition times
- Varying gain steps – nonlinearity; DNL (differential nonlinearity) and INL (integral nonlinearity) similar to ADC and DAC

RF Communications Standards

	Frequency range (MHz)	Channel bandwidth (MHz)	Data rate (Mbps)	Modulation format
802.11b (WLAN)	2400-2500	22	11	CCK
802.11a/g (WLAN)	2400-2500 (g) 5000-6000 (a)	16.8	54	OFDM, 52 subcarriers (4 pilots, 48 data channels)
802.16a (WIMAX)	2000-11000 3 most common bands: 2500, 3400, 5800	1.25-20	Up to 75	OFDM, 256 Subcarriers(200 actually used; 192 are data channels
802.15 (UWB) GSM	3100-10600 3 bands: 890-960 1710-1880 1850-1990	528 0.200	53.3-480 0.270	OFDM GMSK
CDMA 2000	450, 800, 1700, 1900, 2100	1.25	0.060-0.100	CDMA
Bluetooth	2,400-2,500	1		FSK

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Lecture 5: Testing for Distortion

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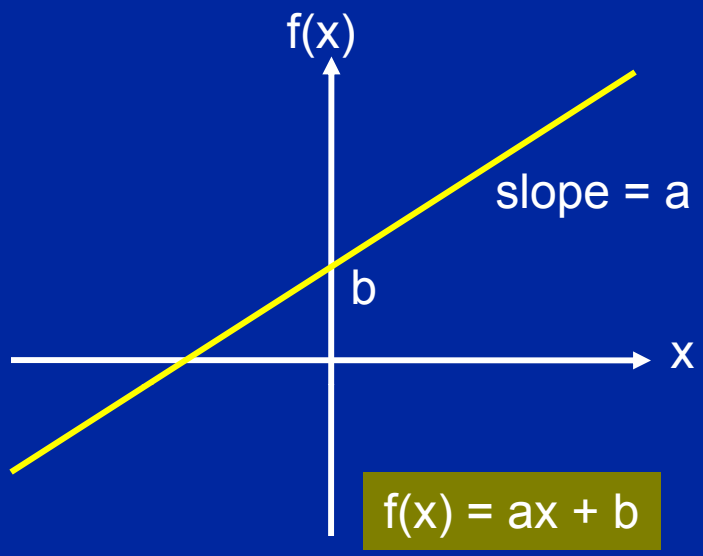
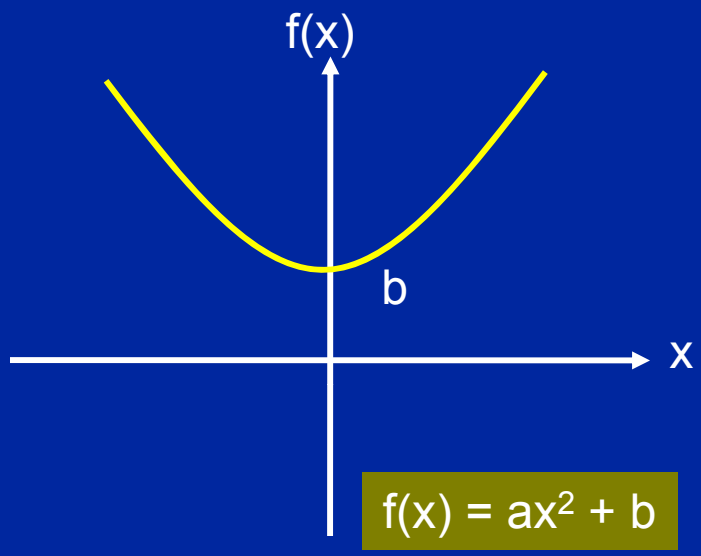
Distortion and Linearity

- An unwanted change in the signal behavior is usually referred to as *distortion*.
- The cause of distortion is nonlinearity of semiconductor devices constructed with diodes and transistors.
- Linearity:
  - Function f(x) = ax + b, although a straight-line is not referred to as a linear function.
  - Definition: A linear function must satisfy:
    - f(x + y) = f(x) + f(y), and
    - f(ax) = a f(x), for all scalar constants a

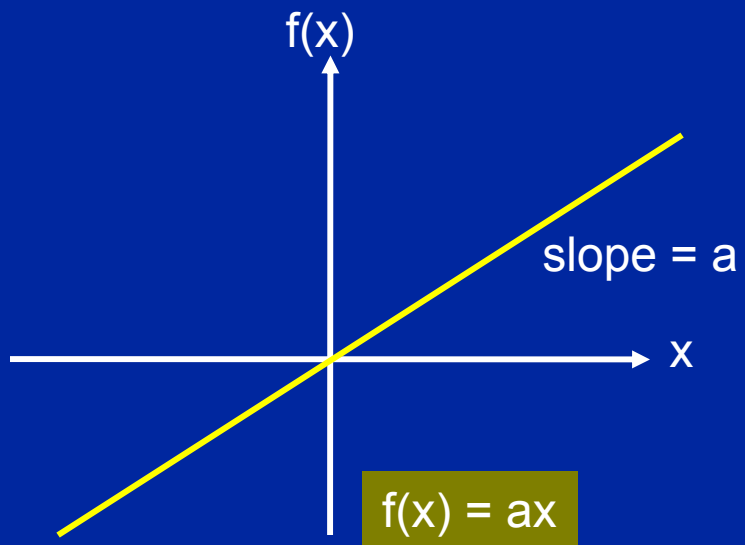
Linear and Nonlinear Functions



$f(x) = ax + b$



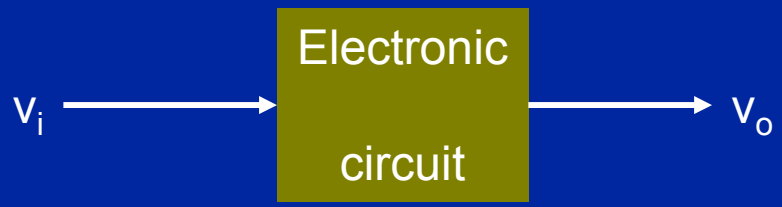
$f(x) = ax^2 + b$



$f(x) = ax$

Generalized Transfer Function

- Transfer function of an electronic circuit is, in general, a nonlinear function.
- Can be represented as a polynomial:
  - $v_o = a_0 + a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + \cdots$
  - Constant term a_0 is the dc component that in RF circuits is usually removed by a capacitor or high-pass filter.
  - For a linear circuit, $a_2 = a_3 = \cdots = 0$.



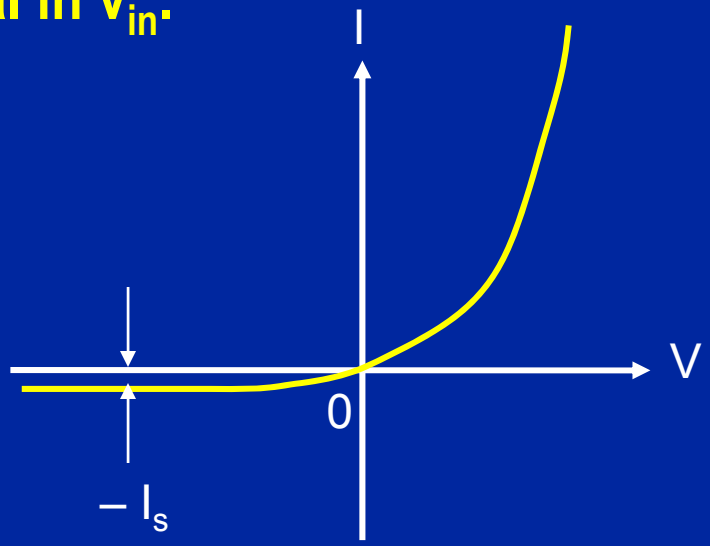
Effect of Nonlinearity on Frequency

- Consider a transfer function, $v_o = a_0 + a_1 v_i + a_2 v_i^2 + a_3 v_i^3$
- Let $v_i = A \cos \omega t$
- Using the identities ($\omega = 2\pi f$):
  - $\cos^2 \omega t = (1 + \cos 2\omega t)/2$
  - $\cos^3 \omega t = (3 \cos \omega t + \cos 3\omega t)/4$
- We get,

$$v_o = a_0 + a_2 A^2/2 + (a_1 A + 3a_3 A^3/4) \cos \omega t + (a_2 A^2/2) \cos 2\omega t + (a_3 A^3/4) \cos 3\omega t$$

Problem for Solution

- A diode characteristic is, $I = I_s (e^{\alpha V} - 1)$
- Where, $V = V_0 + v_{in}$, V_0 is dc voltage and v_{in} is small signal ac voltage. I_s is saturation current and α is a constant that depends on temperature and the design parameters of diode.
- Using the Taylor series expansion, express the diode current I as a polynomial in v_{in}.



Linear and Nonlinear Circuits and Systems

- Linear devices:
  - All frequencies in the output of a device are related to input by a proportionality, or weighting factor, independent of power level.
  - No frequency will appear in the output, that was not present in the input.
- Nonlinear devices:
  - A true linear device is an idealization. Most electronic devices are nonlinear.
  - Nonlinearity in amplifier is undesirable and causes distortion of signal.
  - Nonlinearity in mixer or frequency converter is essential.

Types of Distortion and Their Tests

- Types of distortion:
  - Harmonic distortion: single-tone test
  - Gain compression: single-tone test
  - Intermodulation distortion: two-tone or multitone test
    - Source intermodulation distortion (SIMD)
    - Cross Modulation
- Testing procedure: Output spectrum measurement

Harmonic Distortion

- Harmonic distortion is the presence of multiples of a fundamental frequency of interest. *N* times the fundamental frequency is called *N*th harmonic.
- Disadvantages:
  - Waste of power in harmonics.
  - Interference from harmonics.
- Measurement:
  - Single-frequency input signal applied.
  - Amplitudes of the fundamental and harmonic frequencies are analyzed to quantify distortion as:
    - Total harmonic distortion (THD)
    - Signal, noise and distortion (SINAD)

Problem for Solution

- Show that for a nonlinear device with a single frequency input of amplitude A, the nth harmonic component in the output always contains a term proportional to A^n.

Total Harmonic Distortion (THD)

- THD is the total power contained in all harmonics of a signal expressed as percentage (or ratio) of the fundamental signal power.
- $THD(\%) = [(P_2 + P_3 + \cdots) / P_{fundamental}] \times 100\%$
- Or $THD(\%) = [(V_2^2 + V_3^2 + \cdots) / V^2_{fundamental}] \times 100\%$
  - Where P_2, P_3, . . . , are the power in watts of second, third, . . . , harmonics, respectively, and $P_{fundamental}$ is the fundamental signal power,
  - And V_2, V_3, . . . , are voltage amplitudes of second, third, . . . , harmonics, respectively, and $V_{fundamental}$ is the fundamental signal amplitude.
- Also, THD(dB) = 10 log THD(%)
- For an ideal distortionless signal, THD = 0% or $-\infty$ dB

THD Measurement

- THD is specified typically for devices with RF output.
- The fundamental and harmonic frequencies together are often beyond the bandwidth of the measuring instrument.
- Separate power measurements are made for the fundamental and each harmonic.
- THD is tested at specified power level because
  - THD may be small at low power levels.
  - Harmonics appear when the output power of an RF device is raised.

Signal, Noise and Distortion (SINAD)

- SINAD is an alternative to THD. It is defined as

$$\text{SINAD (dB)} = 10 \log_{10} [(S + N + D)/(N + D)]$$

where

  - S = signal power in watts
  - N = noise power in watts
  - D = distortion (harmonic) power in watts

- SINAD is normally measured for baseband signals.

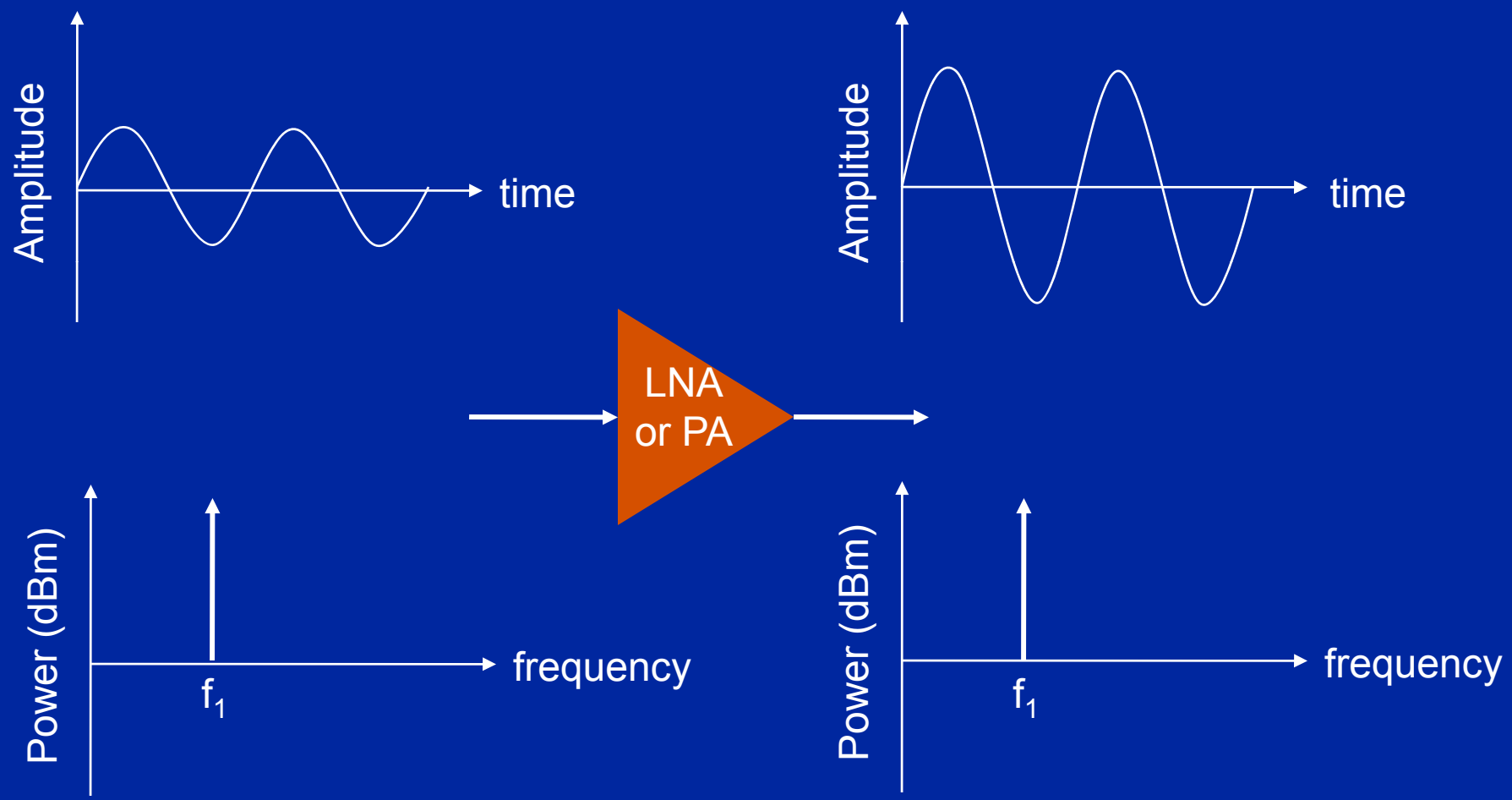
Problems for Solution

- Show that SINAD (dB) > 0.
- Show that for a signal with large noise and high distortion, SINAD (dB) approaches 0.
- Show that for any given noise power level, as distortion increases SINAD will drop.
- For a noise-free signal show that SINAD (dB) = ∞ in the absence of distortion.

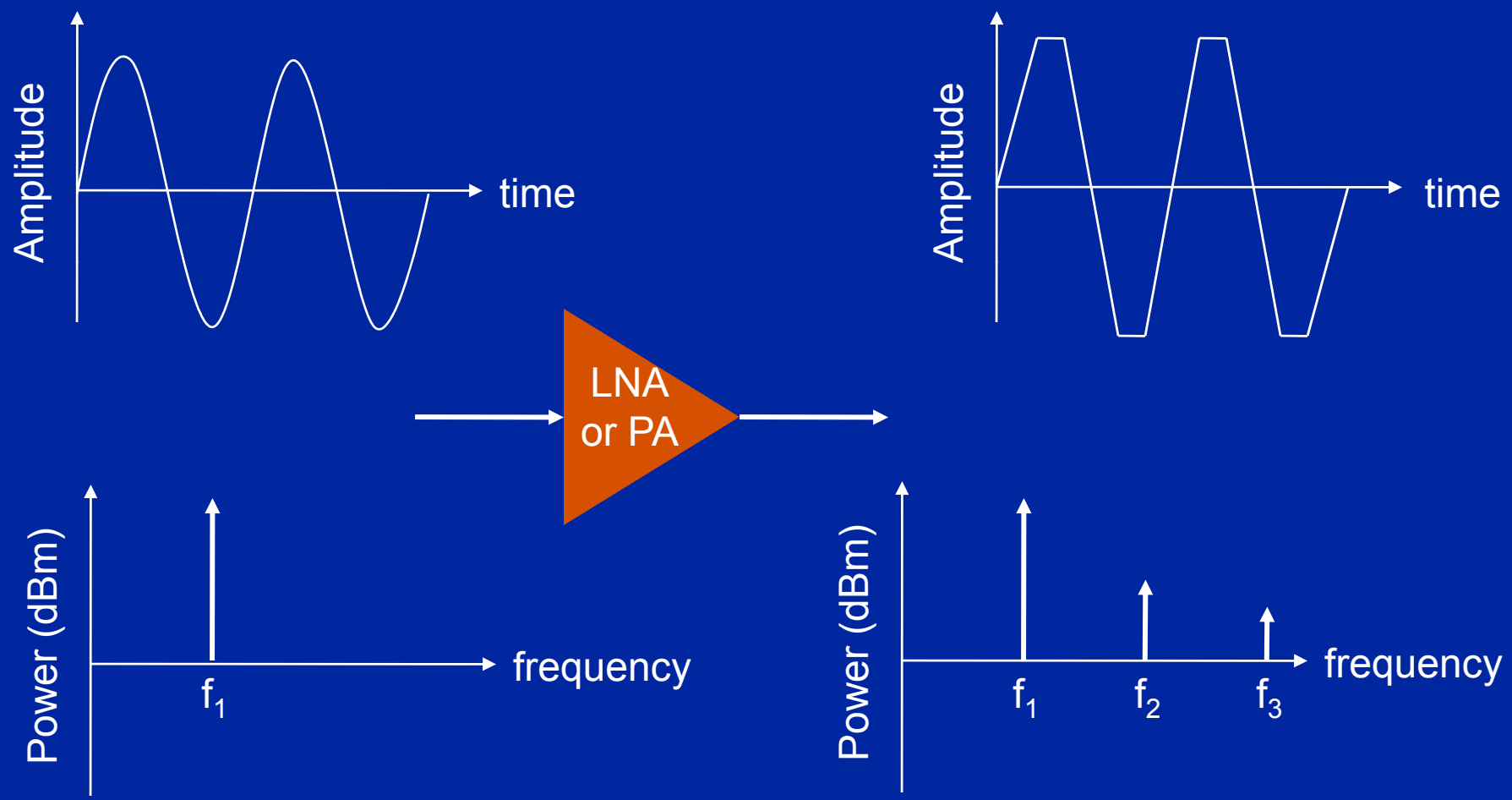
Gain Compression

- The harmonics produced due to nonlinearity in an amplifier reduce the fundamental frequency power output (and gain). This is known as *gain compression*.
- As input power increases, so does nonlinearity causing greater gain compression.
- A standard measure of Gain compression is "1-dB compression point" power level P_{1dB}, which can be
  - *Input referred* for receiver, or
  - *Output referred* for transmitter

Linear Operation: No Gain Compression



Cause of Gain Compression: Clipping



Effect of Nonlinearity

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- Let $v_i = A \cos \omega t$
- Using the identities ($\omega = 2\pi f$):
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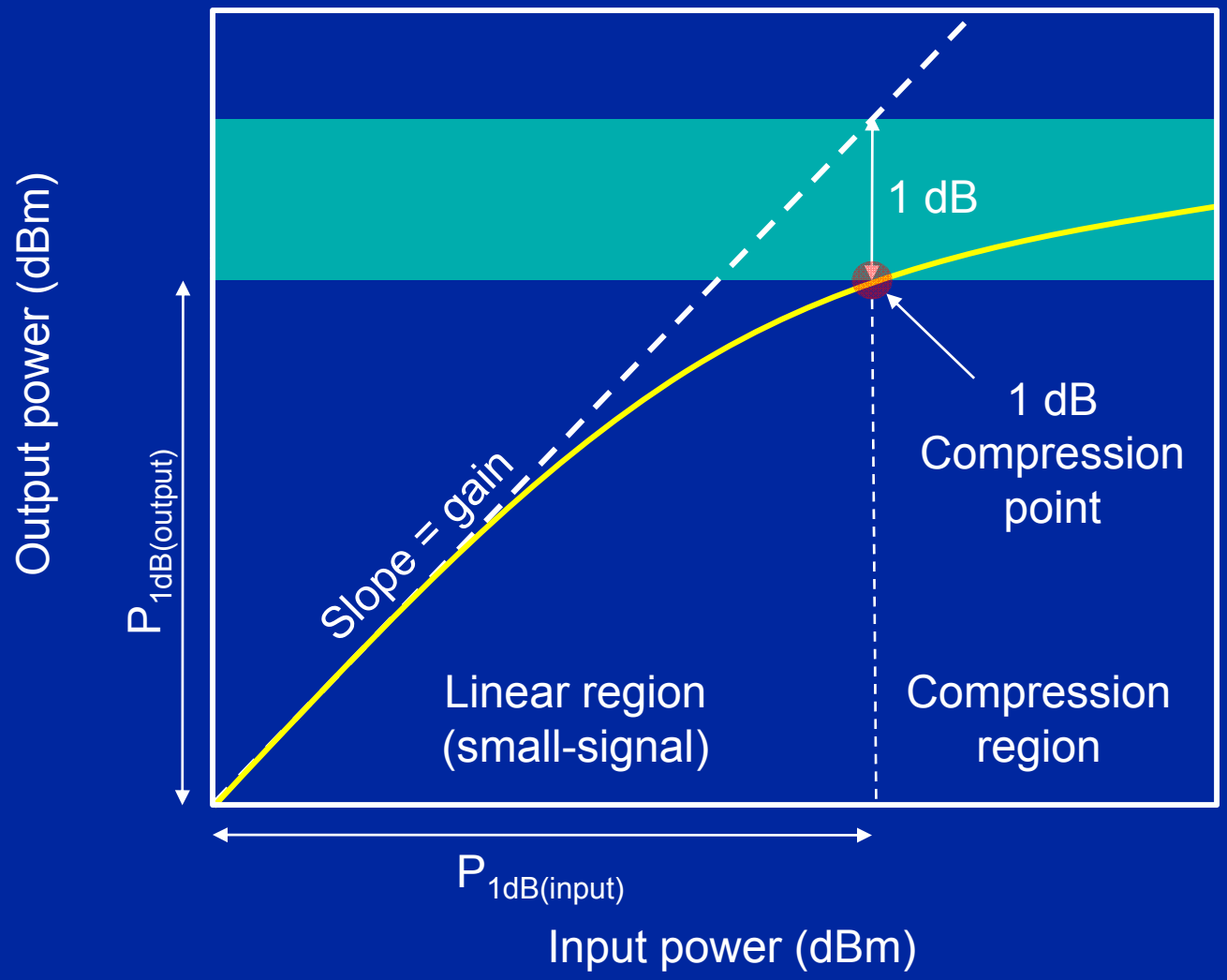
- We get,
  - $v_o = a_0 + a_2 A^2/2 + (a_1 A + 3a_3 A^3/4) \cos \omega t + (a_2 A^2/2) \cos 2\omega t + (a_3 A^3/4) \cos 3\omega t$

Gain Compression Analysis

- DC term is filtered out.
- For small-signal input, A is small
  - A^2 and A^3 terms are neglected
  - $v_o = a_1 A \cos \omega t$, small-signal gain, $G_0 = a_1$
- Gain at 1-dB compression point, $G_{1dB} = G_0 - 1$
- Input referred and output referred 1-dB power:

$$P_{1dB(output)} - P_{1dB(input)} = G_{1dB} = G_0 - 1$$

1-dB Compression Point



Testing for Gain Compression

- Apply a single-tone input signal:
  1. Measure the gain at a power level where DUT is linear.
  2. Extrapolate the linear behavior to higher power levels.
  3. Increase input power in steps, measure the gain and compare to extrapolated values.
  4. Test is complete when the gain difference between steps 2 and 3 is 1dB.
- Alternative test: After step 2, conduct a binary search for 1-dB compression point.

Example: Gain Compression Test

- Small-signal gain, $G_0 = 28\text{dB}$
- Input-referred 1-dB compression point power level,

  $P_{1\text{dB(input)}} = -19\ \text{dBm}$
- We compute:
  - 1-dB compression point Gain, $G_{1\text{dB}} = 28 - 1 = 27\ \text{dB}$
  - Output-referred 1-dB compression point power level,

$$P_{1\text{dB(output)}} = P_{1\text{dB(input)}} + G_{1\text{dB}}$$
$$= -19 + 27$$
$$= 8\ \text{dBm}$$

Intermodulation Distortion

- Intermodulation distortion is relevant to devices that handle multiple frequencies.
- Consider an input signal with two frequencies ω_1 and ω_2:

$$v_i = A \cos \omega_1 t + B \cos \omega_2 t$$

- Nonlinearity in the device function is represented by

$$v_o = a_0 + a_1 v_i + a_2 v_i^2 + a_3 v_i^3$$ *neglecting higher order terms*

- Therefore, device output is

$$v_o = a_0 + a_1 (A \cos \omega_1 t + B \cos \omega_2 t)$$ *DC and fundamental*

$$+ a_2 (A \cos \omega_1 t + B \cos \omega_2 t)^2$$ *2nd order terms*

$$+ a_3 (A \cos \omega_1 t + B \cos \omega_2 t)^3$$ *3rd order terms*

Problems to Solve

- Derive the following:

$$v_o = a_0 + a_1 (A \cos \omega_1 t + B \cos \omega_2 t)$$
$$+ a_2 [A^2 (1+\cos \omega_1 t)/2 + AB \cos (\omega_1+\omega_2)t + AB \cos (\omega_1 - \omega_2)t$$
$$+ B^2 (1+\cos \omega_2 t)/2]$$
$$+ a_3 (A \cos \omega_1 t + B \cos \omega_2 t)^3$$

- Hint: Use the identity:
  - $\cos \alpha \cos \beta = [\cos(\alpha + \beta) + \cos(\alpha - \beta)] / 2$
- Simplify $a_3 (A \cos \omega_1 t + B \cos \omega_2 t)^3$

Two-Tone Distortion Products

- Order for distortion product $mf_1 \pm nf_2$ is $|m| + |n|$

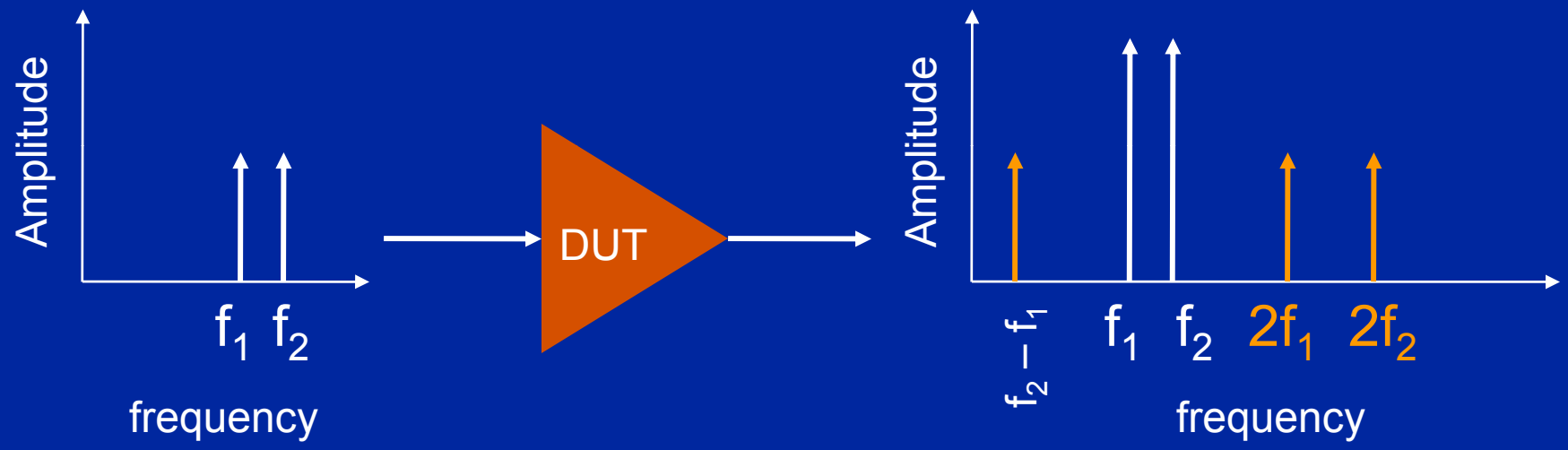
Nunber of distortion products				Frequencies	
Order	Harmonic	Intermod.	Total	Harmonic	Intrmodulation
2	2	2	4	$2f_1$, $2f_2$	$f_1 + f_2$, $f_2 - f_1$
3	2	4	6	$3f_1$, $3f_2$	$2f_1 \pm f_2$, $2f_2 \pm f_1$
4	2	6	8	$4f_1$, $4f_2$	$2f_1 \pm 2f_2$, $2f_2 - 2f_1$, $3f_1 \pm f_2$, $3f_2 \pm f_1$
5	2	8	10	$5f_1$, $5f_2$	$3f_1 \pm 2f_2$, $3f_2 \pm 2f_1$, $4f_1 \pm f_2$, $4f_2 \pm f_1$
6	2	10	12	$6f_1$, $6f_2$	$3f_1 \pm 3f_2$, $3f_2 - 3f_1$, $5f_1 \pm f_2$, $5f_2 \pm f_1$, $4f_1 \pm 2f_2$, $4f_2 \pm 2f_1$
7	2	12	14	$7f_1$, $7f_2$	$4f_1 \pm 3f_2$, $4f_2 - 3f_1$, $5f_1 \pm 2f_2$, $5f_2 \pm 2f_1$, $6f_1 \pm f_2$, $6f_2 \pm f_1$
N	2	2N – 2	2N	Nf_1 , Nf_2	. . . . .

Problem to Solve

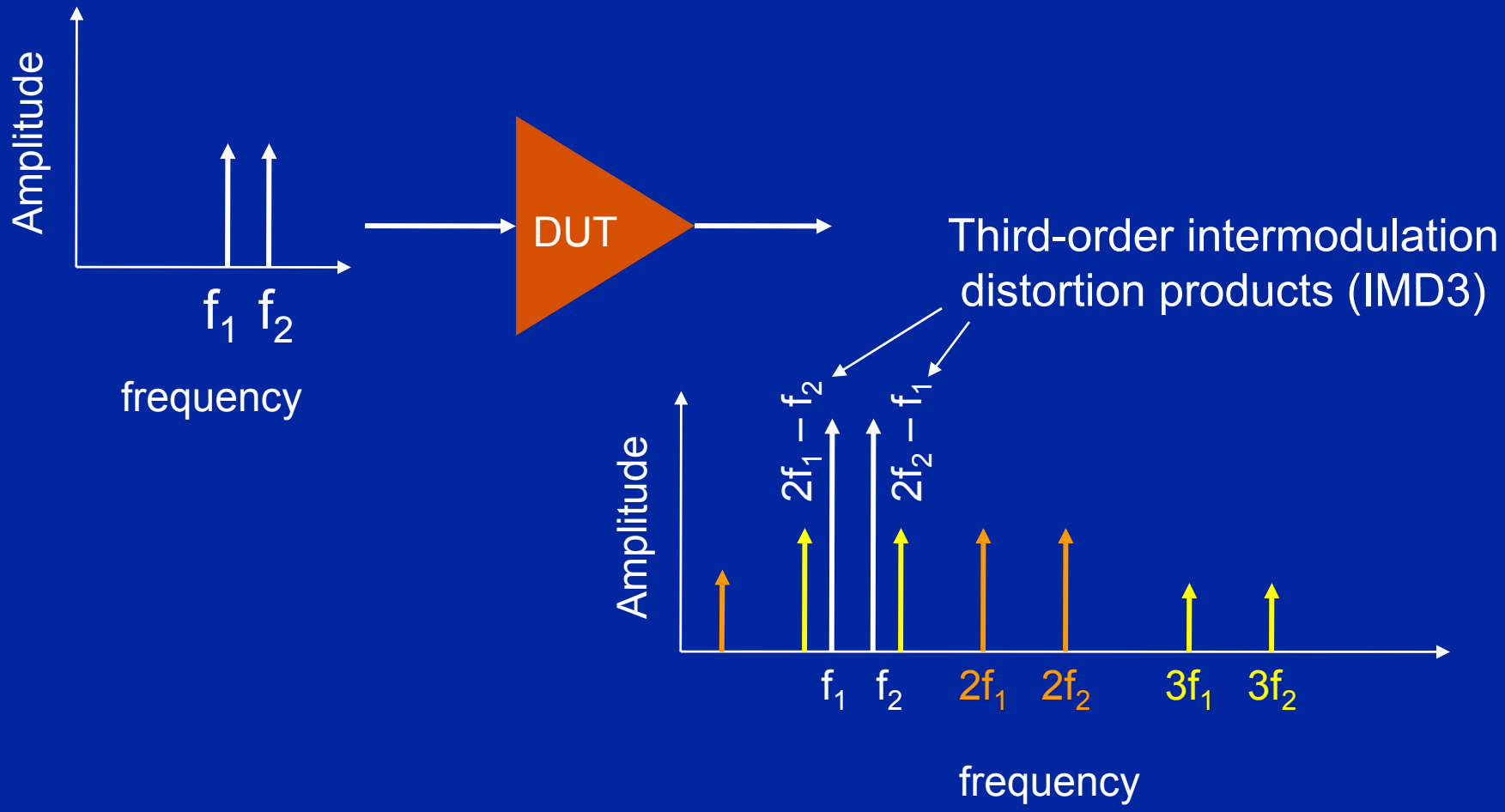
Write Distortion products for two tones 100MHz and 101MHz		
Order	Harmonics (MHz)	Intermodulation products (MHz)
2	200, 202	1, 201
3	300, 3003	**99, 102**, 301, 302
4	400, 404	2, 199, 203, 401, 402, 403
5	500, 505	**98, 103**, 299, 304, 501, 503, 504
6	600, 606	3, 198, 204, 399, 400, 405, 601, 603, 604, 605
7	700, 707	**97, 104**, 298, 305, 499, 506, 701, 707, 703, 704, 705, 706

Intermodulation products close to input tones are shown in **bold.**

Second-Order Intermodulation Distortion



Higher-Order Intermodulation Distortion



Problem to Solve

- For A = B, i.e., for two input tones of equal magnitudes, show that:
  - Output amplitude of each fundamental frequency, f_1 or f_2 , is

$$a_1 A + \frac{9}{4} a_3 A^3$$

  - Output amplitude of each third-order intermodulation frequency, $2f_1 - f_2$ or $2f_2 - f_1$, is

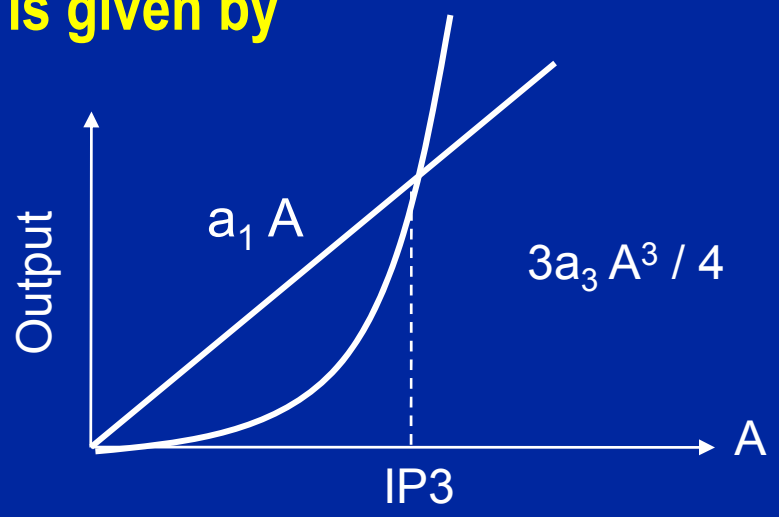
$$\frac{3}{4} a_3 A^3$$

Third-Order Intercept Point (IP3)

- IP3 is the power level of the fundamental for which the output of each fundamental frequency equals the output of the closest third-order intermodulation frequency.
- IP3 is a figure of merit that quantifies the third-order intermodulation distortion.
- Assuming $a_1 >> 9a_3 A^2/4$, IP3 is given by

$$a_1 IP3 = 3a_3 IP3^3 / 4$$

$$IP3 = [4a_1 /(3a_3)]^{1/2}$$



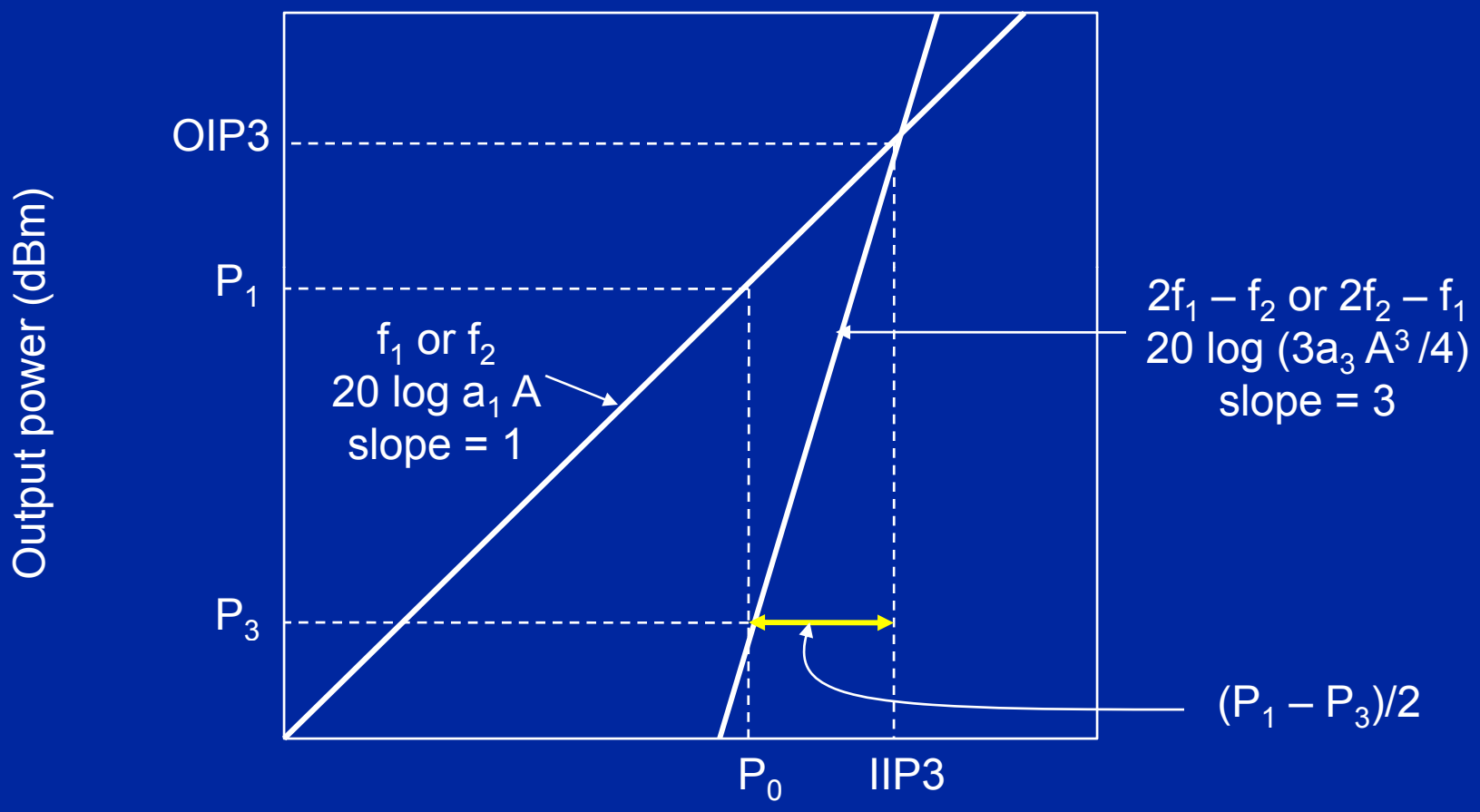
Test for IP3

- Select two test frequencies, f_1 and f_2, applied in equal magnitude to the input of DUT.
- Increase input power P_0 (dBm) until the third-order products are well above the noise floor.
- Measure output power P_1 in dBm at any fundamental frequency and P_3 in dBm at a third-order intermodulation frquency.
- Output-referenced IP3: $OIP3 = P_1 + (P_1 - P_3) / 2$
- Input-referenced IP3: $IIP3 = P_0 + (P_1 - P_3) / 2$

$= OIP3 - G$

Because, Gain for fundamental frequency, $G = P_1 - P_0$

IP3 Graph


Output power (dBm)
OIP3
P_1
P_3
f_1 or f_2
20 log a_1 A
slope = 1
$2f_1 - f_2$ or $2f_2 - f_1$
20 log ($3a_3$ A^3 /4)
slope = 3
$(P_1 - P_3)/2$
P_0
IIP3
Input power = 20 log A dBm

Example: IP3 of an RF LNA

- Gain of LNA = 20 dB
- RF signal frequencies: 2140.10MHz and 2140.30MHz
- Second-order intermodulation distortion: 400MHz; outside operational band of LNA.
- Third-order intermodulation distortion: 2140.50MHz; within the operational band of LNA.
- Test:
  - Input power, P_0 = – 30 dBm, for each fundamental frequency
  - Output power, P_1 = – 30 + 20 = – 10 dBm
  - Measured third-order intermodulation distortion power, P_3 = – 84 dBm
  - OIP3 = – 10 + [(– 10 – (– 84))] / 2 = + 27 dBm
  - IIP3 = – 10 + [(– 10 – (– 84))] / 2 – 20 = + 7 dBm

Source Intermodulation Distortion (SIMD)

- When test input to a DUT contains multiple tones, the input may contain intermodulation distortion known as SIMD.
- Caused by poor isolation between the two sources and nonlinearity in the combiner.
- SIMD should be at least 30dB below the expected intermodulation distortion of DUT.

Cross Modulation

- Cross modulation is the intermodulation distortion caused by multiple carriers within the same bandwidth.
- Examples:
  - In cable TV, same amplifier is used for multiple channels.
  - Orthogonal frequency division multiplexing (OFDM) used in WiMAX or WLAN use multiple carriers within the bandwidth of the same amplifier.
- Measurement:
  - Turn on all tones/carriers except one
  - Measure the power at the frequency that was not turned on
- B. Ko, et al., "A Nightmare for CDMA RF Receiver: The Cross Modulation," Proc. 1st IEEE Asia Pacific Conf. on ASICs, Aug. 1999, pp. 400-402.

RFIC Design and Testing for Wireless Communications

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July 23, 2008

Lecture 6: Testing for Noise

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What is Noise?

- Noise in an RF system is unwanted random fluctuations in a desired signal.
- Noise is a natural phenomenon and is always present in the environment.
- Effects of noise:
  - Interferes with detection of signal (hides the signal).
  - Causes errors in information transmission by changing signal.
  - Sometimes noise might imitate a signal falsely.
- All communications system design and operation must account for noise.

Describing Noise

- Consider noise as a random voltage or current function, x(t), over interval – T/2 < t < T/2.
- Fourier transform of x(t) is $X_T(f)$.
- Power spectral density (PSD) of noise is power across 1Ω

$$S_x(f) = \lim_{T \to \infty} \left[E\{ |X_T(f)|^2 \} / (2T) \right] \quad \text{volts}^2/\text{Hz}$$

This is also expressed in dBm/Hz.

Thermal Noise

- Thermal (Johnson) noise: Caused by random movement of electrons due to thermal energy that is proportional to temperature.
- Called white noise due to uniform PSD over all frequencies.
- Mean square open circuit noise voltage across R Ω resistor [Nyquist, 1928]:

$$v^2 = 4hfBR / [\exp(hf/kT) - 1]$$

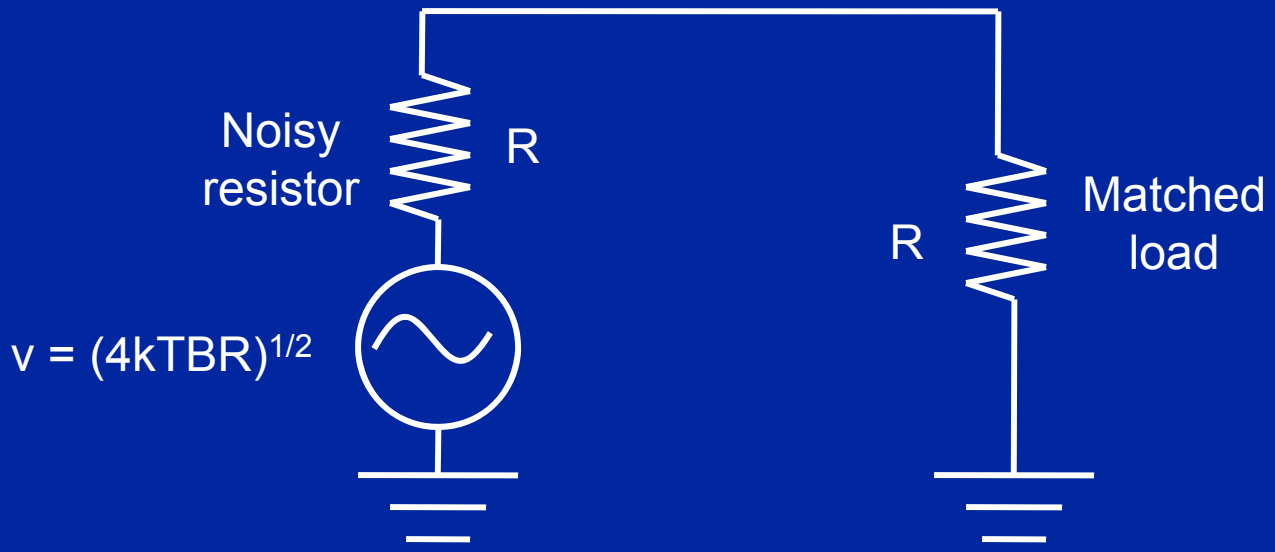
  - Where
    - Plank's constant $h = 6.626 \times 10^{34}$ J-sec
    - Frequency and bandwidth in hertz = f, B
    - Boltzmann's constant $k = 1.38 \times 10^{-23}$ J/K
    - Absolute temperature in Kelvin = T

Problem to Solve

- Given that for microwave frequencies, hf << kT, derive the following Rayleigh-Jeans approximation:

$$v^2 = 4kTBR$$

- Show that at room temperature (T = 290K), thermal noise power supplied by resistor R to a matched load is ktB or – 174 dBm/Hz.



Other Noise Types

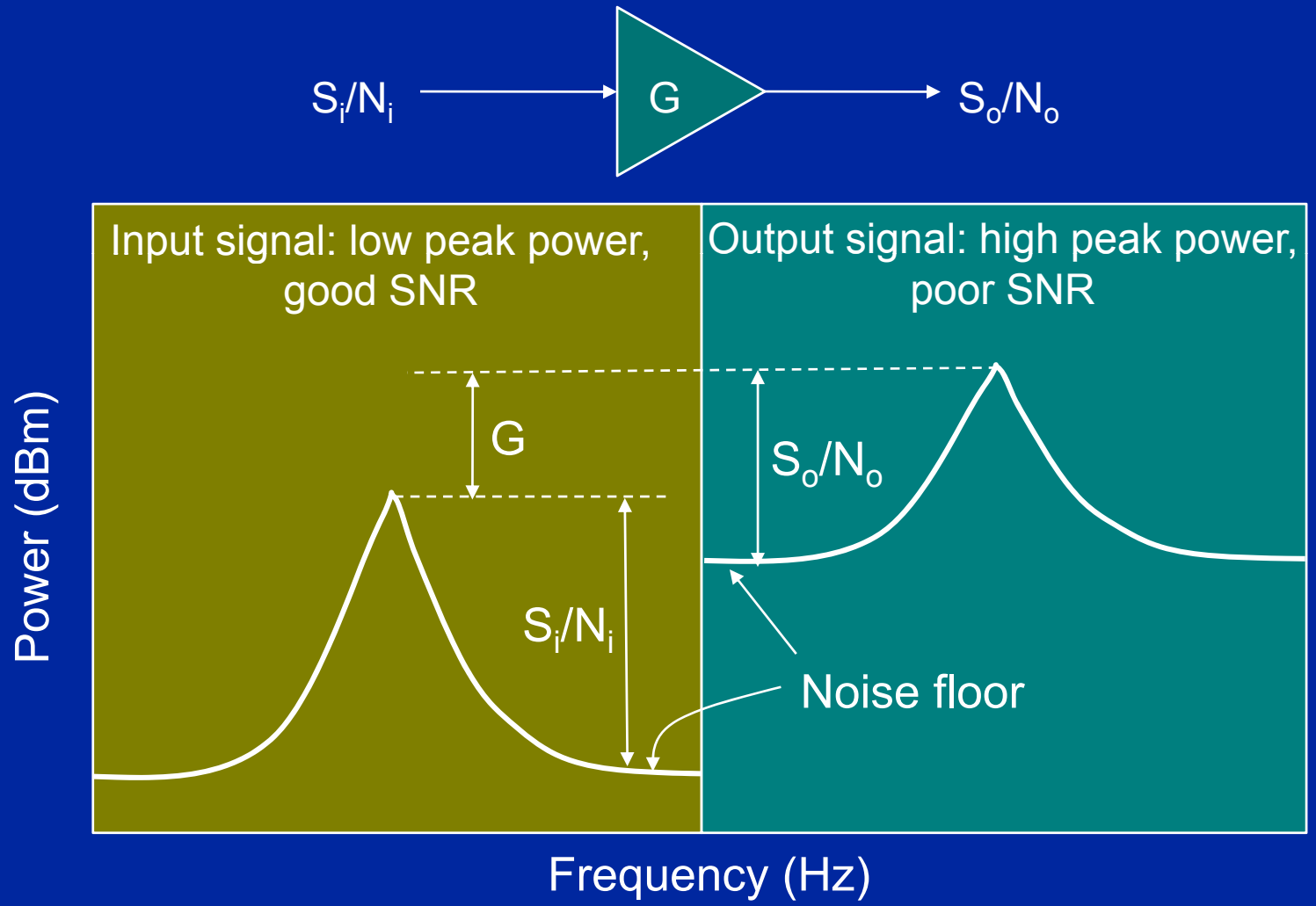
- Shot noise [Schottky, 1928]: Broadband noise due to random behavior of charge carriers in semiconductor devices.
- Flicker (1/f) noise: Low-frequency noise in semiconductor devices, perhaps due to material defects; power spectrum falls off as 1/f. Can be significant at audio frequencies.
- Quantization noise: Caused by conversion of continuous valued analog signal to discrete-valued digital signal; minimized by using more digital bits.
- Quantum noise: Broadband noise caused by the quantized nature of charge carriers; significant at very low temperatures (~0K) or very high bandwidth ($> 10^{15}$ Hz).
- Plasma noise: Caused by random motion of charges in ionized medium, possibly resulting from sparking in electrical contacts; generally, not a concern.

Measuring Noise

- Expressed as noise power density in the units of dBm/Hz.
- Noise sources:
  - Resistor at constant temperature, noise power = kTB W/Hz.
  - Avalanche diode
- Noise temperature:
  - T_n = (Available noise power in watts)/(kB) kelvins
- Excess noise ratio (ENR) is the difference in the noise output between hot (on) and cold (off) states, normalized to reference thermal noise at room temperature (290K):
  - $ENR = [k(T_h - T_c)B]/(kT_0B) = (T_h / T_0) - 1$
  - Where noise output in cold state is takes same as reference.
  - 10 log ENR ~ 15 to 20 dB

Signal-to-Noise Ratio (SNR)

- **SNR is the ratio of signal power to noise power.**



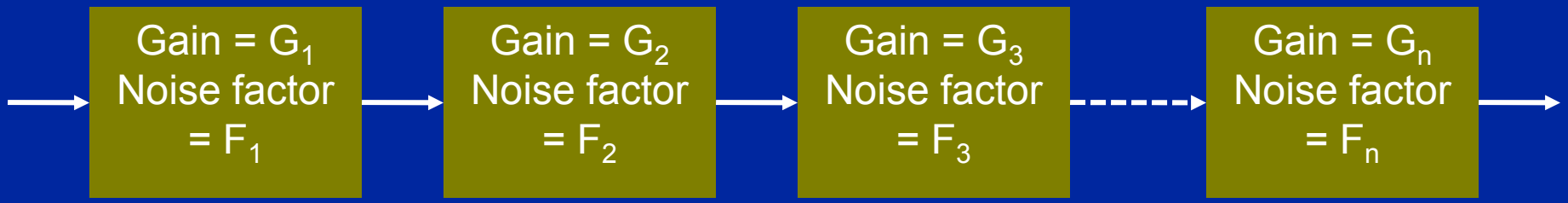
Noise Factor and Noise Figure

- Noise factor (F) is the ratio of input SNR to output SNR:
  - $F = (S_i / N_i) / (S_o / N_o)$
    $= N_o / (GN_i)$ when S_i = 1W and G = gain of DUT
    $= N_o /(kT_0 BG)$ when $N_i = kT_0 B$ for input noise source
  - $F \geq 1$
- Noise figure (NF) is noise factor expressed in dB:
  - $NF = 10 \log F$ dB
  - $0 \leq NF \leq \infty$

Cascaded System Noise Factor

- **Friis equation [Proc. IRE, July 1944, pp. 419 – 422]:**

$$F_{sys} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \cdots G_{n-1}}$$



Measuring Noise Figure: Cold Noise Method

- Example: SOC receiver with large gain so noise output is measurable; noise power should be above noise floor of measuring equipment.
- Gain G is known or previously measured.
- Noise factor, $F = N_o / (kT_0BG)$, where
  - N_o is measured output noise power (noise floor)
  - B is measurement bandwidth
  - At 290K, $kT_0 = -174$ dBm/Hz
- Noise figure, NF = 10 log F

  $= N_o\,(dB) - (-174\ dBm/Hz) - B(dB) - G(dB)$
- This measurement is also done using S-parameters.

Y – Factor

- Y – factor is the ratio of output noise in hot (power on) state to that in cold (power off) state.
- $Y = N_h / N_c$

  $= N_h / N_0$
- Y is a simple ratio.
- Consider, $N_h = kT_hBG$ and $N_c = kT_0BG$
- Then $N_h - N_c = kBG(T_h - T_0)$ or $kBG = (N_h - N_c) / (T_h - T_0)$
- Noise factor, $F = N_h /(kT_0 BG) = (N_h / T_0) [1 / (kBG)]$

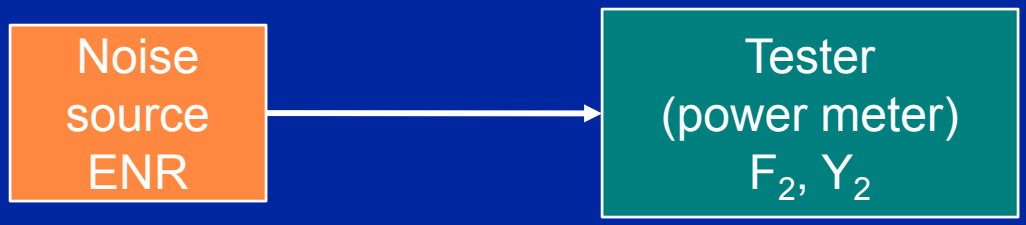
  $= (N_h / T_0) (T_h - T_0) / (N_h - N_c)$

  $= ENR / (Y - 1)$

Measuring Noise Factor: Y – Factor Method

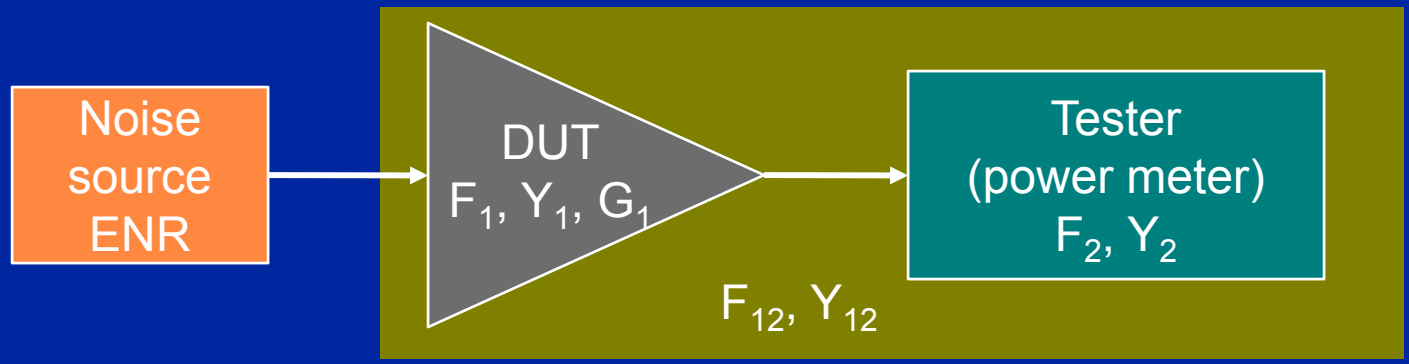
- Noise source provides hot and cold noise power levels and is characterized by ENR (excess noise ratio).
- Tester measures noise power, is characterized by its noise factor F_2 and Y-factor Y_2.
- Device under test (DUT) has gain G_1 and noise factor F_1.
- Two-step measurement:
  - Calibration: Connect noise source to tester, measure output power for hot and cold noise inputs, compute Y_2 and F_2.
  - Measurement: Connect noise source to DUT and tester cascade, measure output power for hot and cold noise inputs, compute compute Y_{12}, F_{12} and G_1.
  - Use Friis equation to obtain F_1.

Calibration



- $Y_2 = N_{h2} / N_{c2}$, where
  - N_{h2} = measured power for hot source
  - N_{c2} = measured power for cold source
- $F_2 = ENR / (Y_2 - 1)$

Cascaded System Measurement



- $Y_{12} = N_{h12} / N_{c12}$, where
  - N_{h12} = measured power for hot source
  - N_{c12} = measured power for cold source
- $F_{12} = ENR / (Y_{12} - 1)$
- $G_1 = (N_{h12} - N_{c12}) / (N_{h2} - N_{c2})$

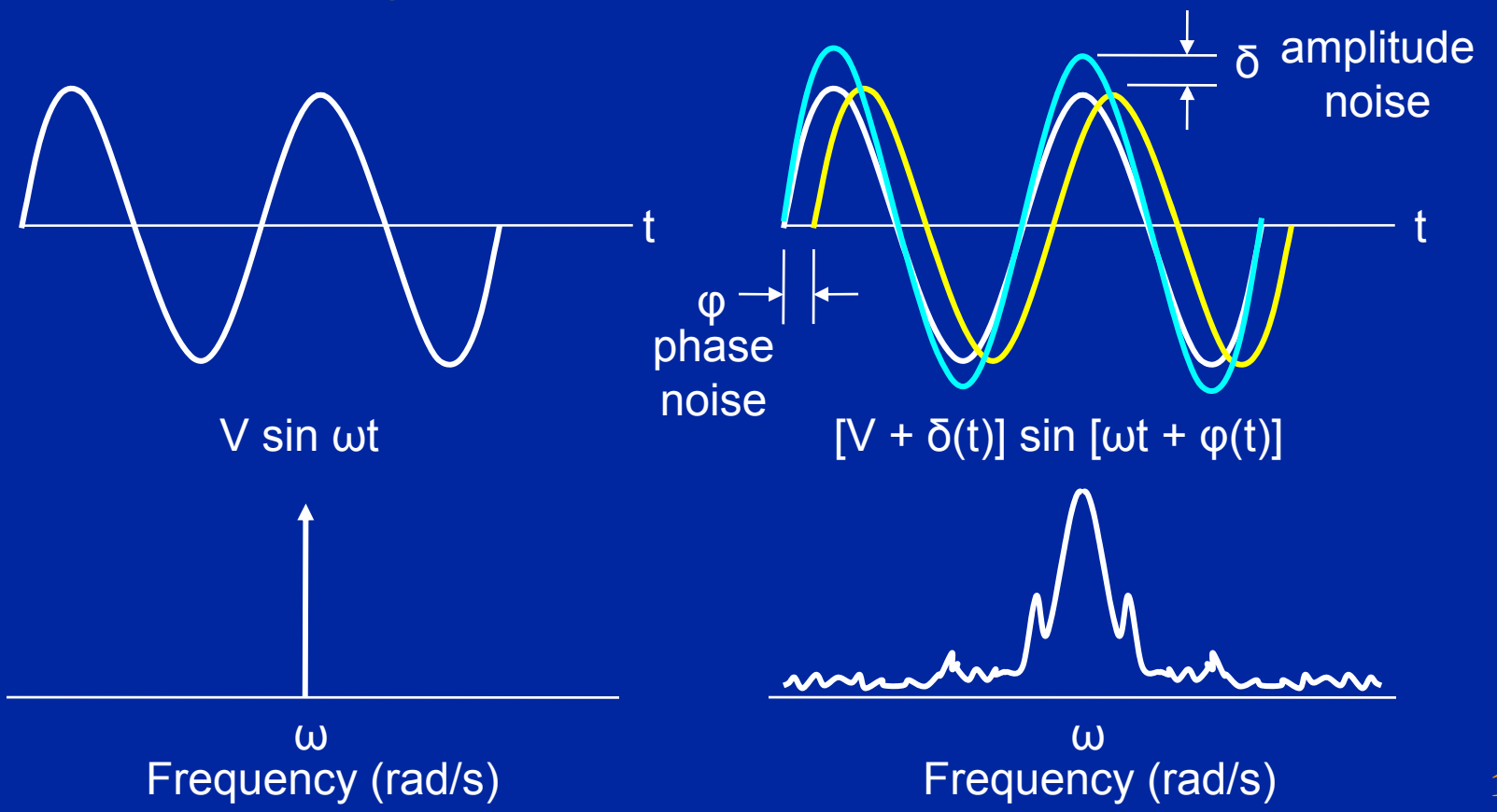
Problem to Solve

- Show that from noise measurements on a cascaded system, the noise factor of DUT is given by

$$F_1 = F_{12} - \frac{F_2 - 1}{G_1}$$

Phase Noise

- Phase noise is due to small random variations in the phase of an RF signal. In time domain, phase noise is referred to as *jitter*.
- Understanding phase:



Effects of Phase Noise

- Similar to phase modulation by a random signal.
- Two types:
  - Long term phase variation is called *frequency drift*.
  - *Sh*ort term phase variation is *phase noise*.
- Definition: Phase noise is the Fourier spectrum (power spectral density) of a sinusoidal carrier signal with respect to the carrier power.

$$L(f) = P_n / P_c \text{ (as ratio)}$$

$$= P_n \text{ in dBm/Hz} - P_c \text{ in dBm (as dBc)}$$

  - P_n is RMS noise power in 1-Hz bandwidth at frequency f
  - P_c is RMS power of the carrier

Phase Noise Analysis

$$[V + \delta(t)] \sin [\omega t + \varphi(t)] = [V + \delta(t)] [\sin \omega t \cos \varphi(t) + \cos \omega t \sin \varphi(t)]$$

$$\approx [V + \delta(t)] \sin \omega t + [V + \delta(t)] \varphi(t) \cos \omega t$$

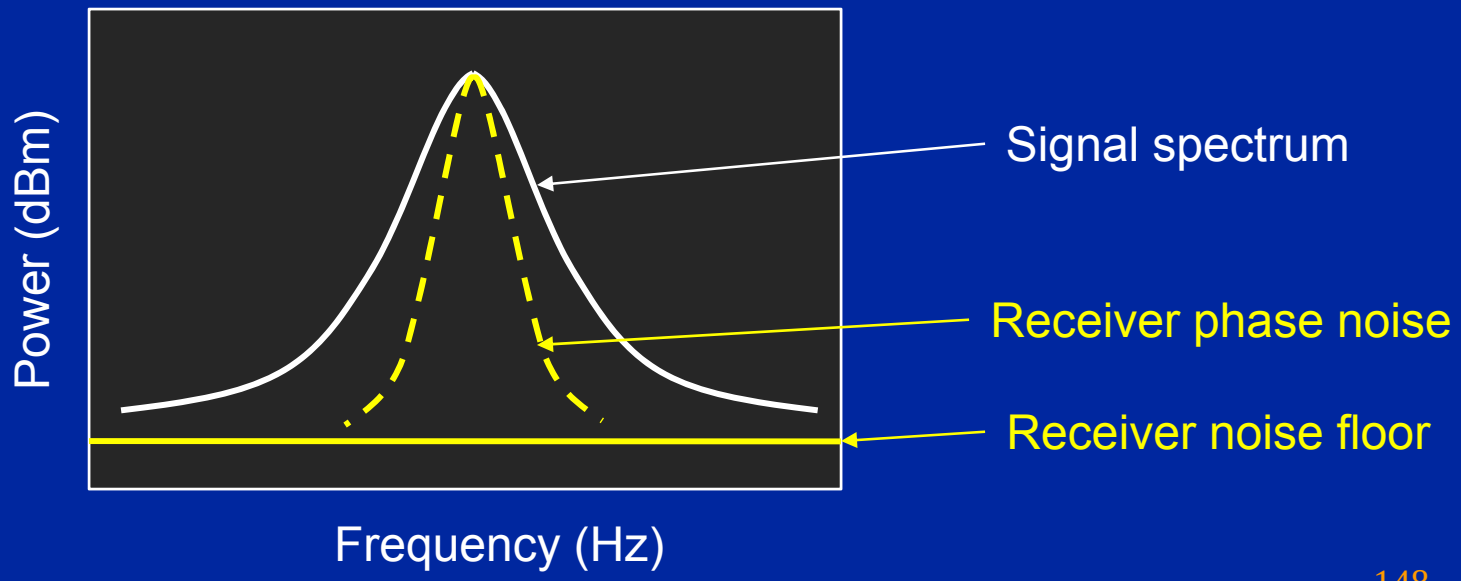
In-phase carrier frequency with amplitude noise
White noise δ(t) corresponds to noise floor

Quadrature-phase carrier frequency with amplitude and phase noise
Short-term phase noise corresponds to phase noise spectrum

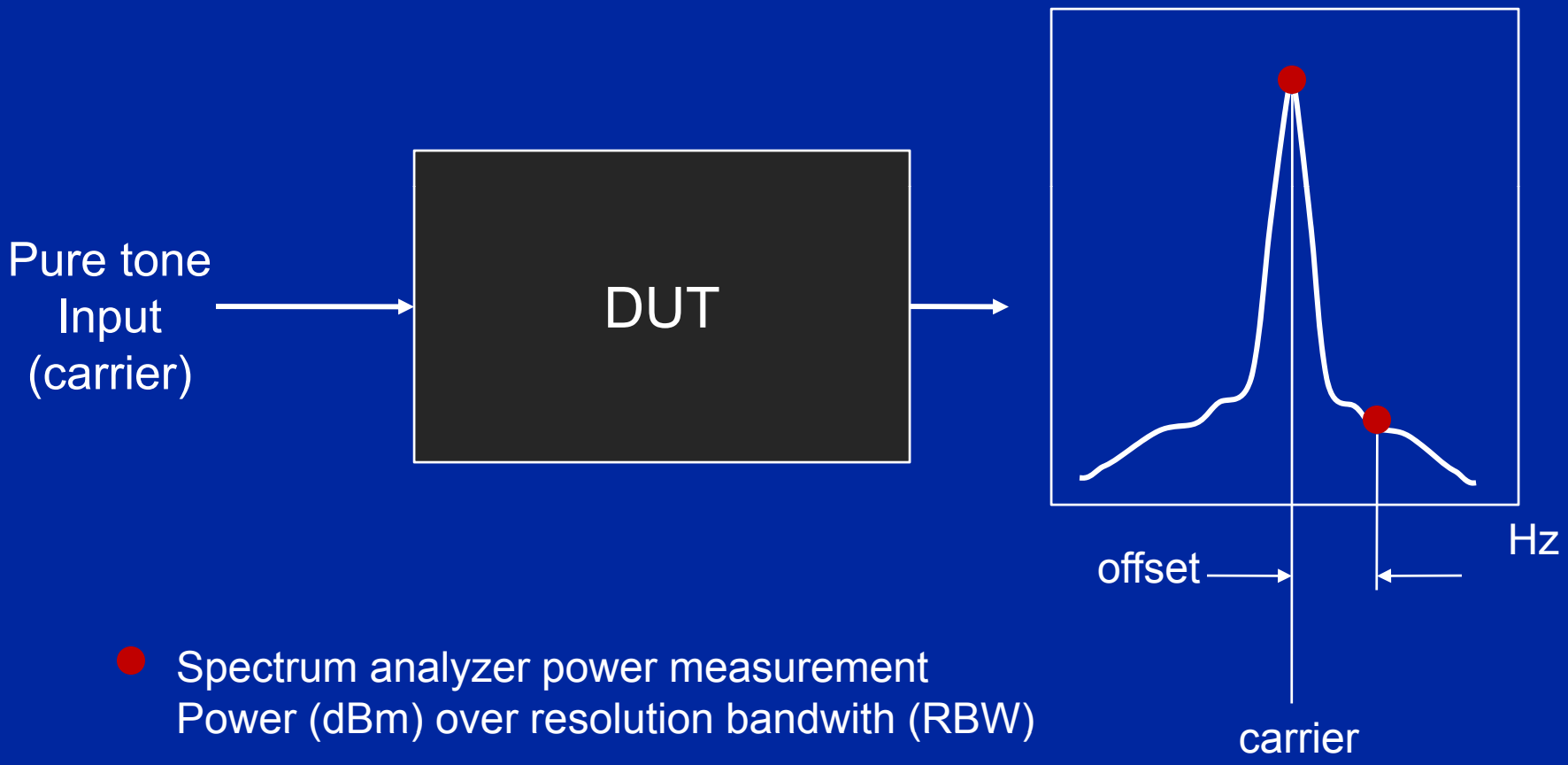
Phase spectrum, $L(f) = S_{\varphi}(f)/2$
Where $S_{\varphi}(f)$ is power spectrum of φ(t)

Phase Noise Measurement

- Phase noise is measured by low noise receiver (amplifier) and spectrum analyzer:
  - Receiver must have a lower noise floor than the signal noise floor.
  - Local oscillator in the receiver must have lower phase noise than that of the signal.



Phase Noise Measurement



- Spectrum analyzer power measurement
  Power (dBm) over resolution bandwith (RBW)

Phase Noise Measurement Example

- Spectrum analyzer data:
  - RBW = 100Hz
  - Frequency offset = 2kHz
  - $P_{carrier}$ = – 5.30 dBm
  - P_{offset} = – 73.16 dBm
- Phase noise, L(f) = $P_{offset} - P_{carrier}$ – 10 log RBW

  = – 73.16 – (– 5.30) – 10 log 100

  = – 87.86 dBc/Hz
- Phase noise is specified as " – 87.86 dBc/Hz at 2kHz from the carrier."

Problem to Solve

- Consider the following spectrum analyzer data:
  - RBW = 10Hz
  - Frequency offset = 2kHz
  - $P_{carrier}$ = – 3.31 dBm
  - P_{offset} = – 81.17 dBm
- Determine phase noise in dBc/Hz at 2kHz from the carrier.

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Lecture 7: ATE and SOC Testing

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Automatic Test Equipment (ATE)

- ATE provides test facility for:
  - Digital and memory devices
  - Analog devices (analog instrumentation)
  - RF devices (AWG – arbitrary waveform generators, LNA, noise source, RF sources, filters, PMU – power measurement units, Spectrum analyzer)
  - Test fixtures, load-boards, handlers
- Cost of ATE: $500,000 to $2M, or higher
- Testing cost of chip ~ 3 – 5 cents/second

Variables in Cost of Testing

- Shifts per day: 3
- Hours per shift: 8
- Yield: 80%
- Utilization: 60% (significant effort for calibration)
- Depreciation: 5 years
- Cost of ATE: $1M
- Cost of handler: $250,000
- Test time: 1.5 seconds
- Handler index time: 1 second

Problem to Solve

- Find the testing cost for a good device shipped using the data given in the previous slide.

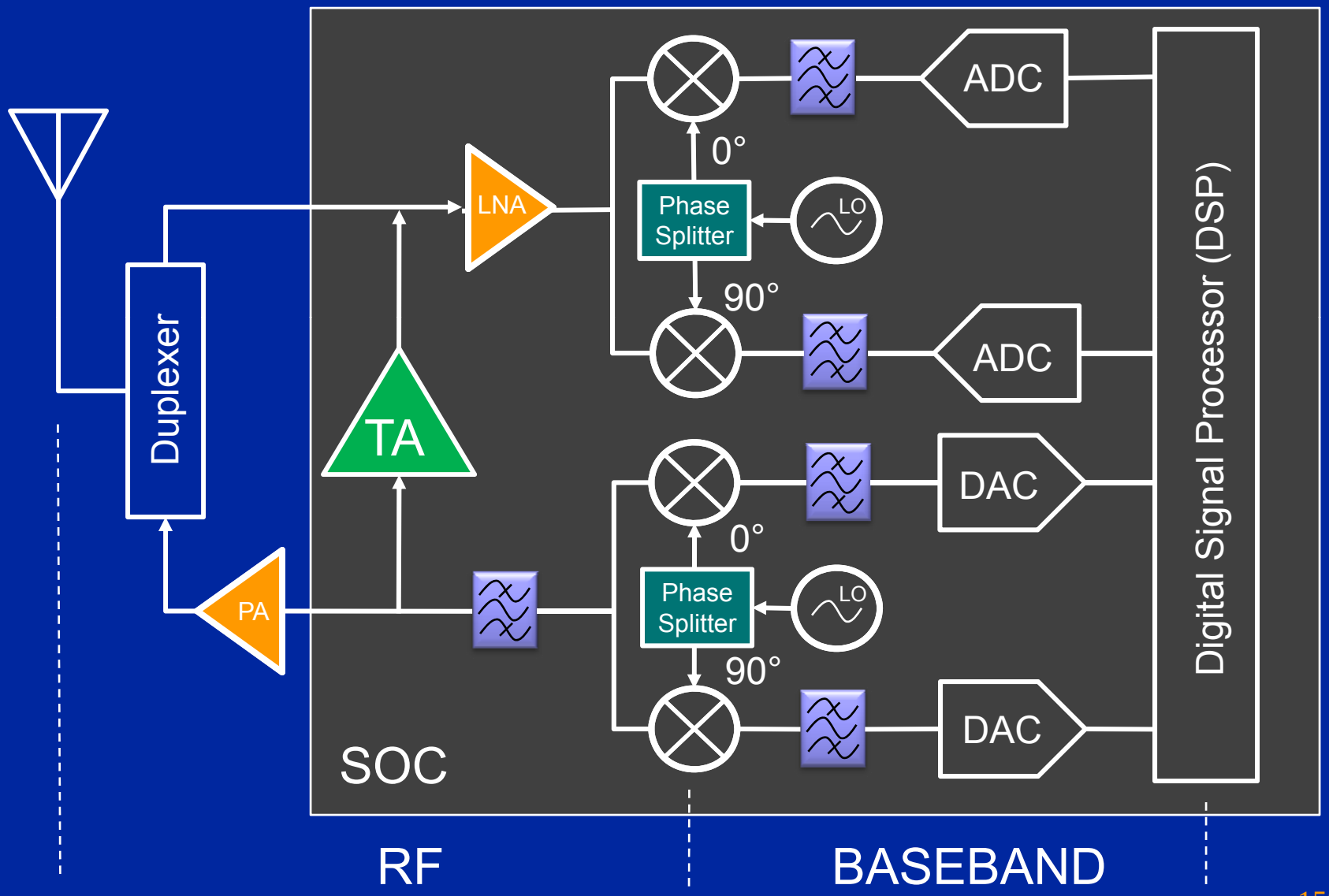
Testing Cost

- Tester time per year:
  - $T = 365 \times 24 \times 3600 \times 0.6 = 18{,}921{,}600$ s
- Number of devices tested per year:
  - $N_T = T/(1.5 + 1.0) = 7{,}568{,}640$
- Number of good devices produced per year:
  - $N = N_T \times \text{Yield} = 7{,}568{,}640 \times 0.8 = 6{,}054{,}912$
- Testing cost per year:
  - $C = (1{,}000{,}000 + 250{,}000)/5 = 250{,}000$ dollars
- Testing cost per device shipped:
  - Cost = C/N = 4.13 cents

Reducing Test Cost

- Ping-pong testing: Use the same ATE with multiple handlers.
- Multisite testing: Test multiple chips together, typically, 4, 16, . . .
- Built-in self-test (BIST): Applicable to SOC and SIP devices.
- Low-cost testers.

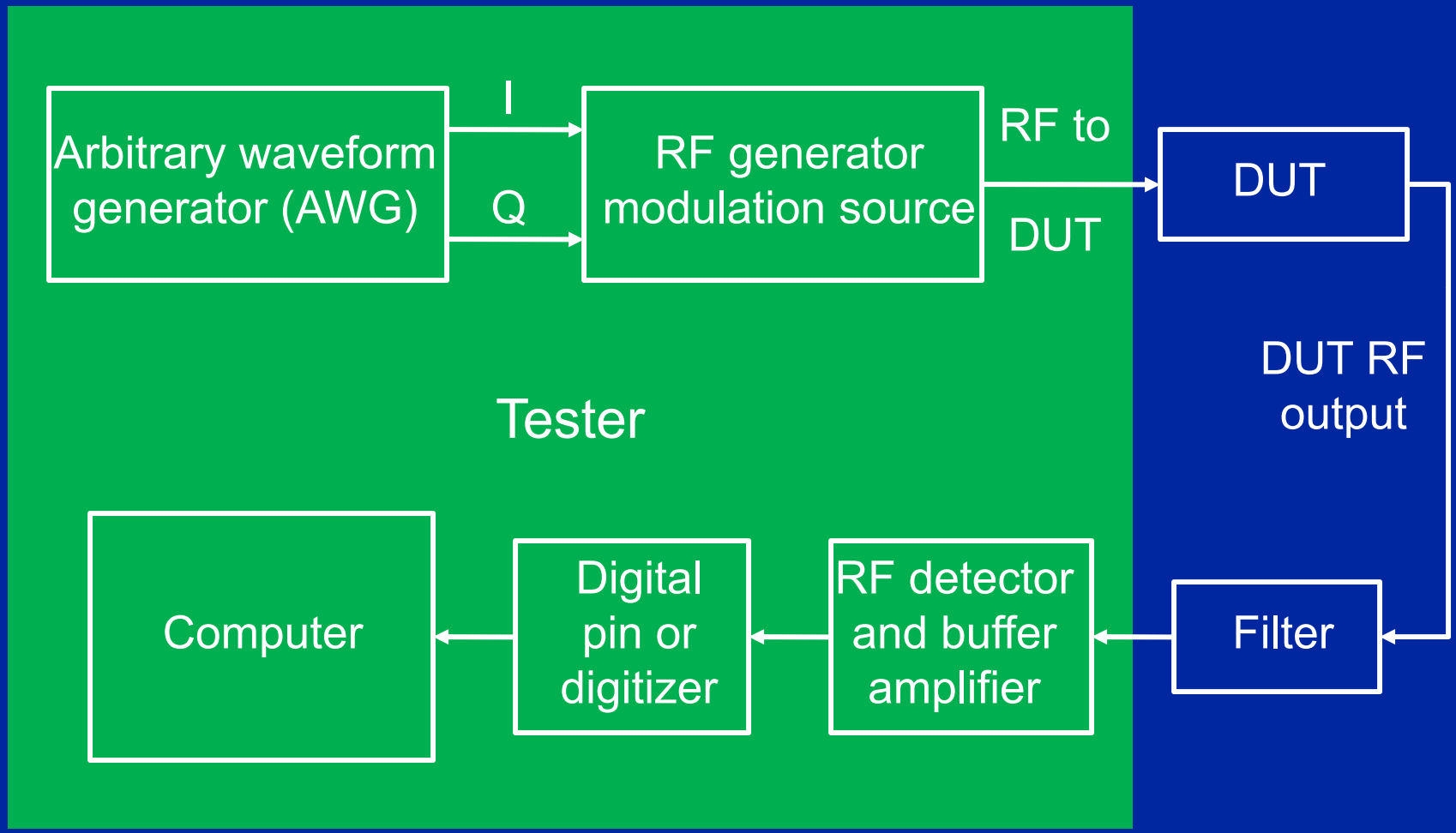
BIST for a SOC ZIF Transceiver



ZIF SOC BIST

- Test implemented at baseband.
- Loopback between A/D and D/A converters.
- DSP implemented with digital BIST.
- Test amplifier (TA) implemented on chip; is disabled during normal operation.
- A test procedure:
  - Test DSP using digital BIST.
  - Apply RF BIST:
    - Pseudorandom bit sequence generated by DSP
    - Upconverted by transmitter chain and applied to receiver through TA
    - Down converted signal compared to input bit sequence by DSP to analyze bit error rate (BER)
    - BER correlated to relevant characteristics of SOC components
- Advantage: Low tester cost. Disadvantage: Poor diagnosis.

Low-Cost Tester for Wideband RF Parameters



References

- **SOC BIST**
  - **J. Dabrowski, "BiST Model for IC RF-Transceiver Front-End,"** *Proc. 18th IEEE International Symp. on Defect and Fault Tolerance in VLSI Systems*, **2003.**
  - **D. Lupea, et al., "RF-BIST: Loopback Spectral Signature Analysis,"** *Proc. Design, Automation and Test in Europe Conf.*, **2003.**
- **BIST for power amplifier**
  - **F. Obaldia, et al., "On-Chip Test Mechanism for Transceiver Power Amplifier and Oscillator Frequency," US Patent No. 20040148121A1, 2004.**
- **Low-cost testing**
  - **F. Goh, et al., "Innovative Technique for Testing Wide Bandwidth Frequency Response," Wireless Broadband Forum, Cambridge, UK, 2004.**

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Lecture 8: RF BIST

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Purpose

- Develop Built-In Self-Test (BIST) approach using direct digital synthesizer (DDS) for functionality testing of analog circuitry in mixed-signal systems
- Provides BIST-based measurement of
  - Amplifier linearity (IP3)
  - Gain and frequency response
- Implemented in hardware
  - IP3, gain, and freq. response measured

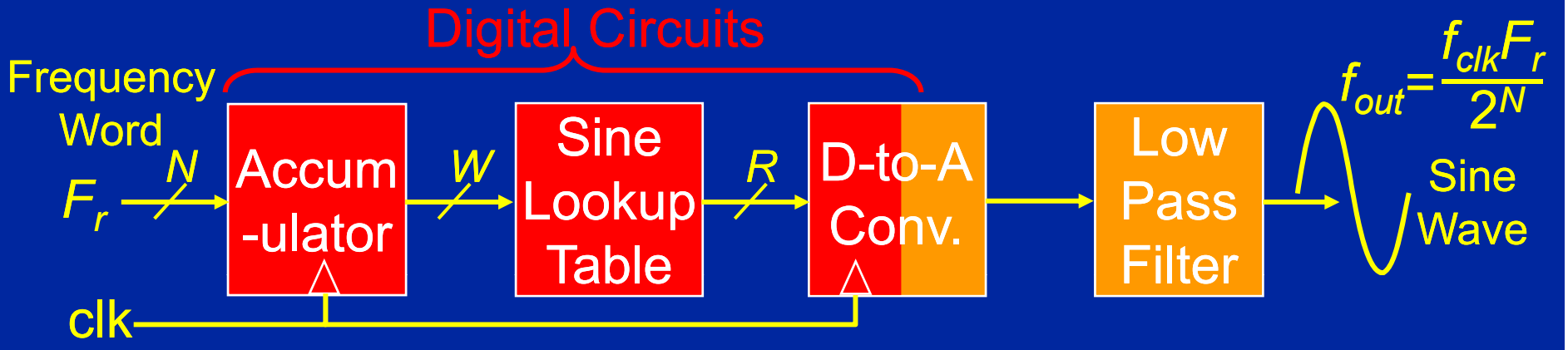
Outline

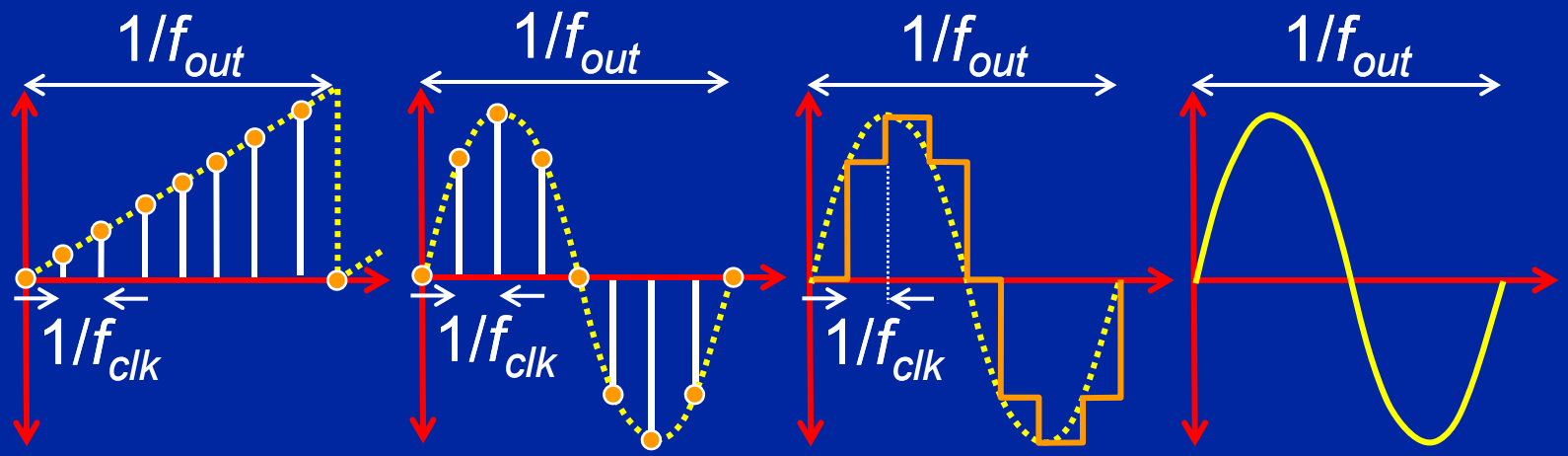
- Overview of direct digital synthesizers (DDS)
- 3rd order inter-modulation product (IP3)
- BIST architecture
  - Test pattern generator
  - Output response analyzer
- Experimental results
  - Implementation in hardware
  - IP3 Measurements

Direct Digital Synthesis (DDS)

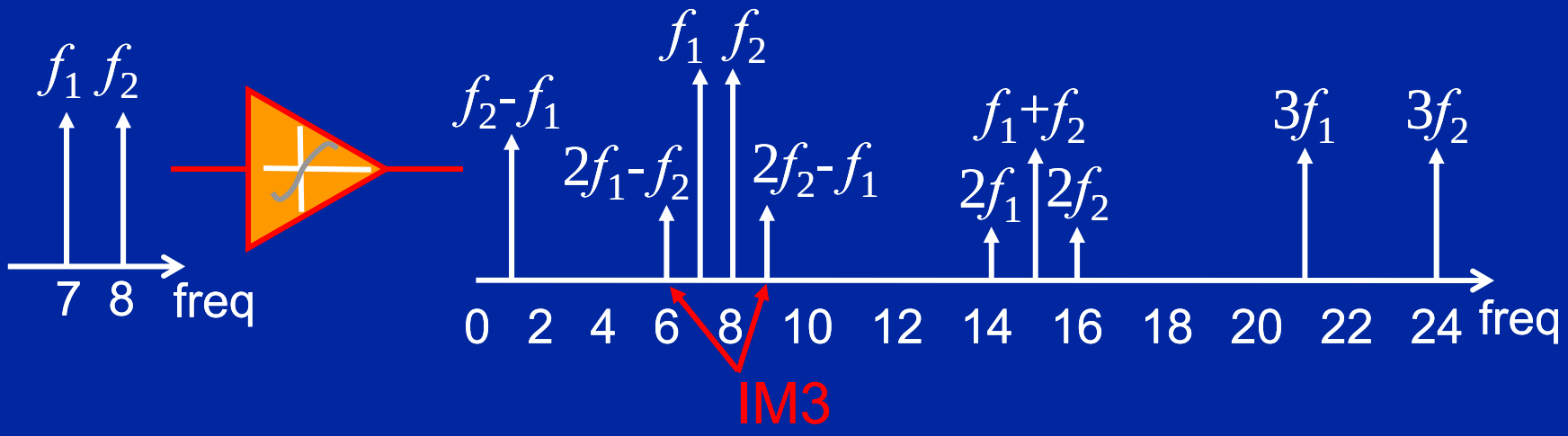
- DDS ⇒ generating deterministic communication carrier/reference signals in discrete time using digital hardware
  - converted into analog signals using a DAC
- Advantages
  - Capable of generating a variety of waveforms
  - High precision ⇒ sub Hz
  - Digital circuitry
    - Small size ⇒ fraction of analog synthesizer size
    - Low cost
    - Easy to implementation

Typical DDS Architecture





Intermodulation



- Two signals with different frequencies are applied to a nonlinear system
  - Output exhibits components that are not harmonics of input fundamental frequencies
- Third-order intermodulation (IM3) is critical
  - Very close to fundamental frequencies

Mathematical Foundation

- **Input 2-tone:**

  $x(t)=A_1\cos\omega_1 t + A_2\cos\omega_2 t$

- **Output of non-linear device:**

  $y(t)=\alpha_0+\alpha_1 x(t)+\alpha_2 x^2(t)+\alpha_3 x^3(t)+\ldots$

- **Substituting $x(t)$ into $y(t)$:**

  $y(t) = \frac{1}{2}\alpha_2(A_1^2+A_2^2)$

  $+ [\alpha_1 A_1+\frac{3}{4}\alpha_3 A_1(A_1^2+2A_2^2)]\cos\omega_1 t + [\alpha_1 A_2+\frac{3}{4}\alpha_3 A_2(2A_1^2+A_2^2)]\cos\omega_2 t$

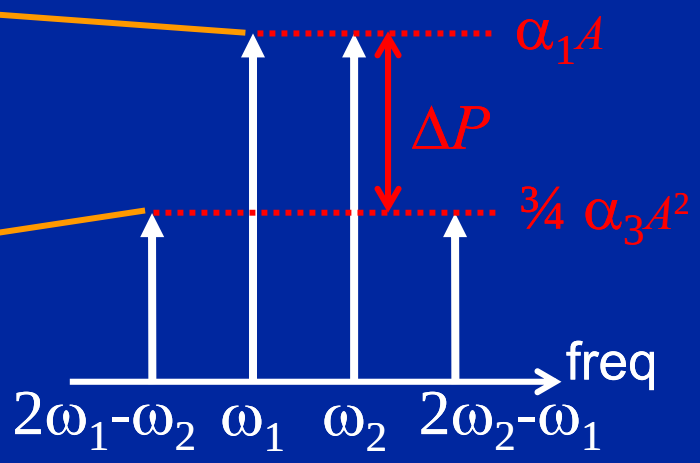
  $+ \frac{1}{2}\alpha_2(A_1^2\cos 2\omega_1 t+A_2^2\cos 2\omega_2 t)$

  $+ \alpha_2 A_1 A_2[\cos(\omega_1+\omega_2)t+\cos(\omega_1-\omega_2)t]$

  $+ \frac{1}{4}\alpha_3[A_1^3\cos 3\omega_1 t+A_2^2\cos 3\omega_2 t]$

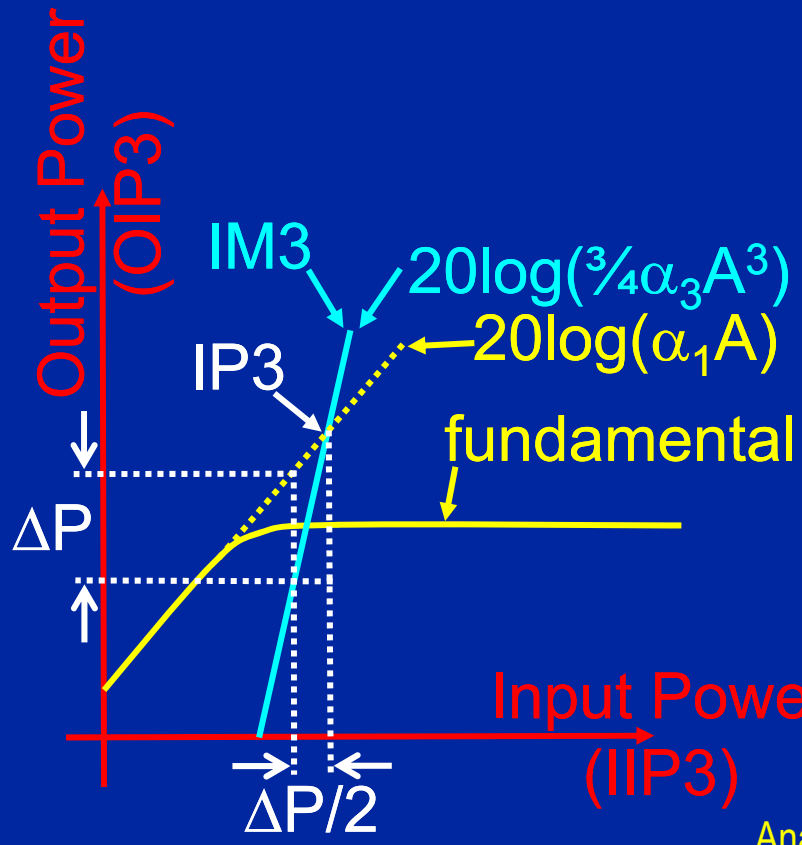
  $+ \frac{3}{4}\alpha_3\{A_1^2A_2[\cos(2\omega_1+\omega_2)t+\cos(2\omega_1-\omega_2)t]$

  $+A_1A_2^2[\cos(2\omega_2+\omega_1)t+\cos(2\omega_2-\omega_1)t]\}$

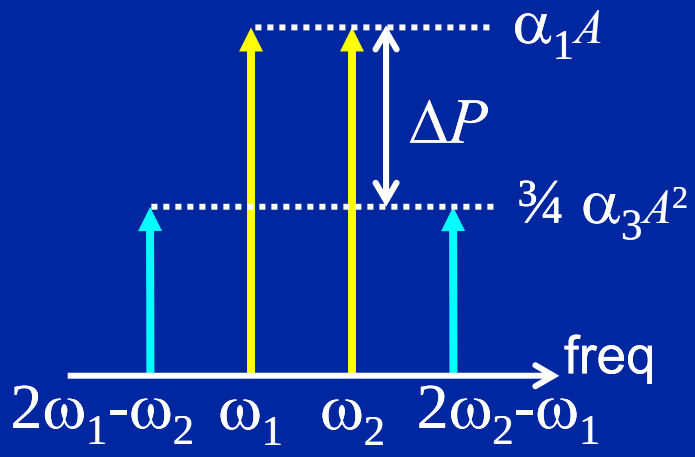


3rd order Intercept Point (IP3)

- IP3 is theoretical input power point where 3rd-order distortion and fundamental output lines intercept
  - $IIP_3[dBm] = \frac{\Delta P[dB]}{2} + P_{in}[dBm]$

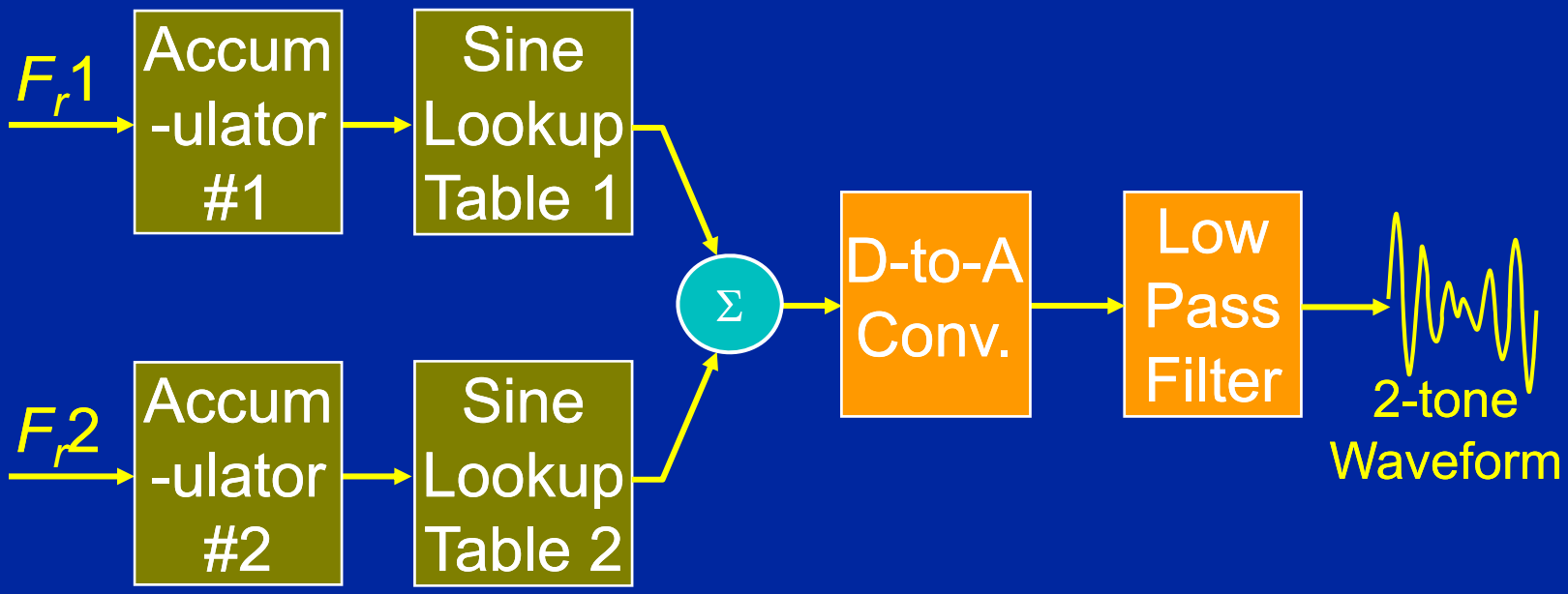


Practical measurement with spectrum analyzer



2-tone Test Pattern Generator

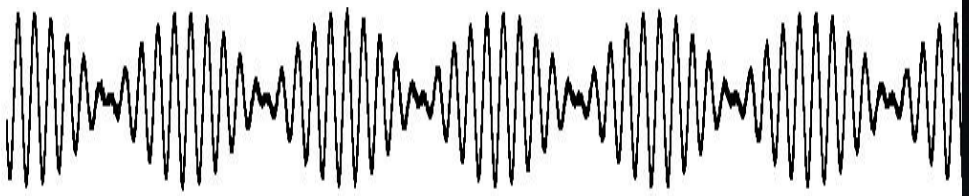
- Two DDS outputs are superimposed using adder to generate 2-tone waveform used for IP3 measurement
- F_r1 and F_r2 control frequencies of 2-tone waveform



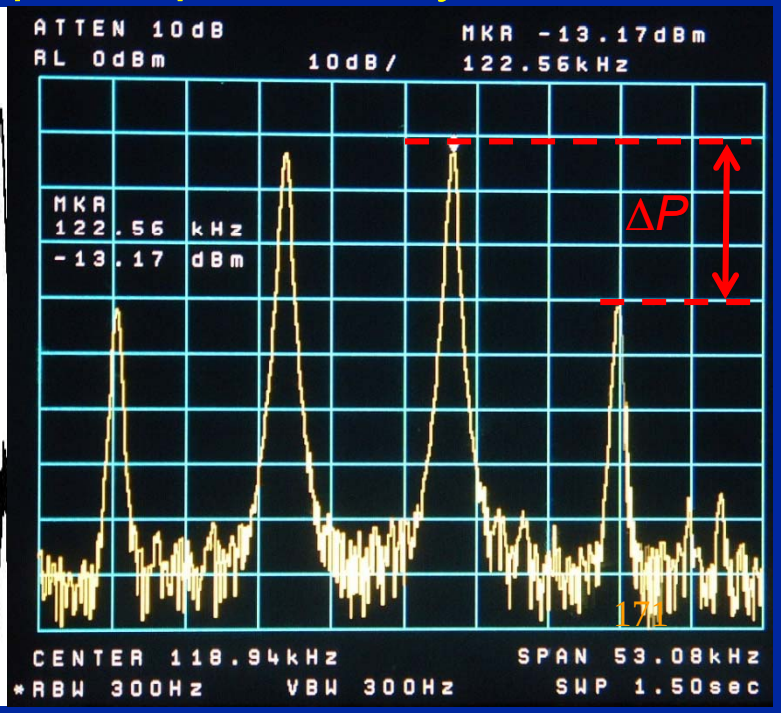
Actual 2-tone IP3 Measurement

- Outputs of DAC and DUT taken with scope from our experimental hardware implementation
- Typical ΔP measurement requires expensive, external spectrum analyzer
  - For BIST we need an efficient output response analyzer

DAC output x(*t*):



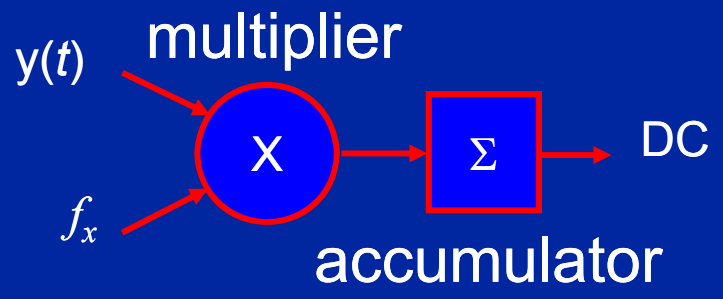
DUT output y(*t*):



Output Response Analyzer

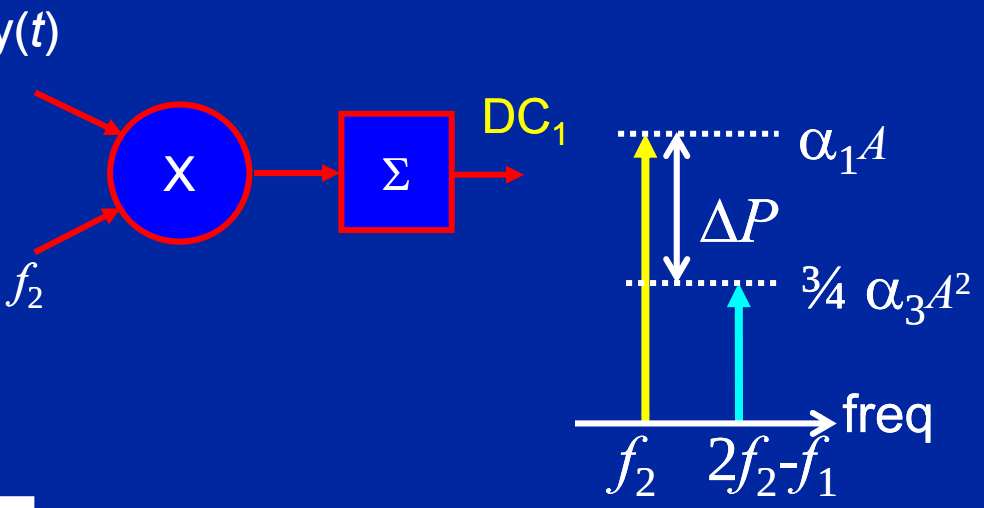
Multiplier/accumulator-based ORA

- Multiply the output response by a frequency
- Accumulate the multiplication result
- Average by # of clock cycles of accumulation
  - Gives DC value proportional to power of signal at that frequency
- Advantages
  - Easy to implement
  - Low area overhead
  - Exact frequency control
  - More efficient than FFT

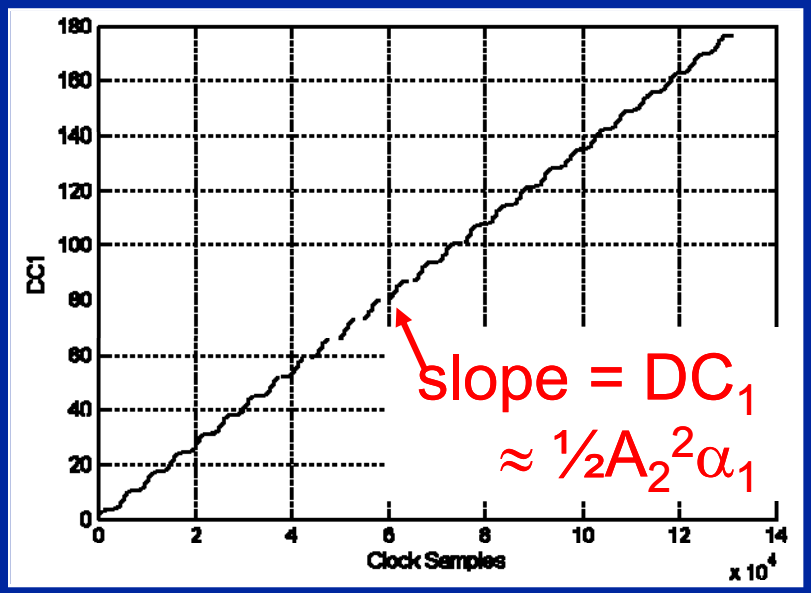


DC_1 Accumulator

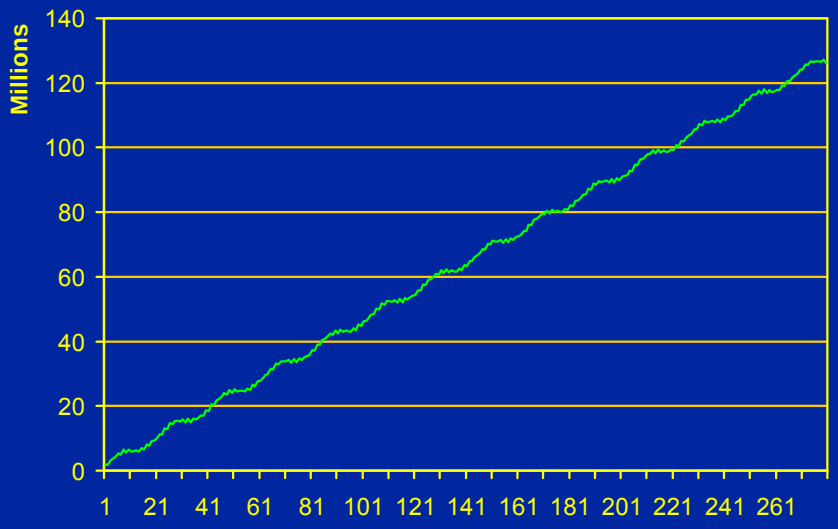
- $y(t) \times f_2 \Rightarrow DC_1 \approx \frac{1}{2}A_2^2\alpha 1$
- Ripple in slope due to low frequency components
  - Longer accumulation reduces effect of ripple



Simulation Results

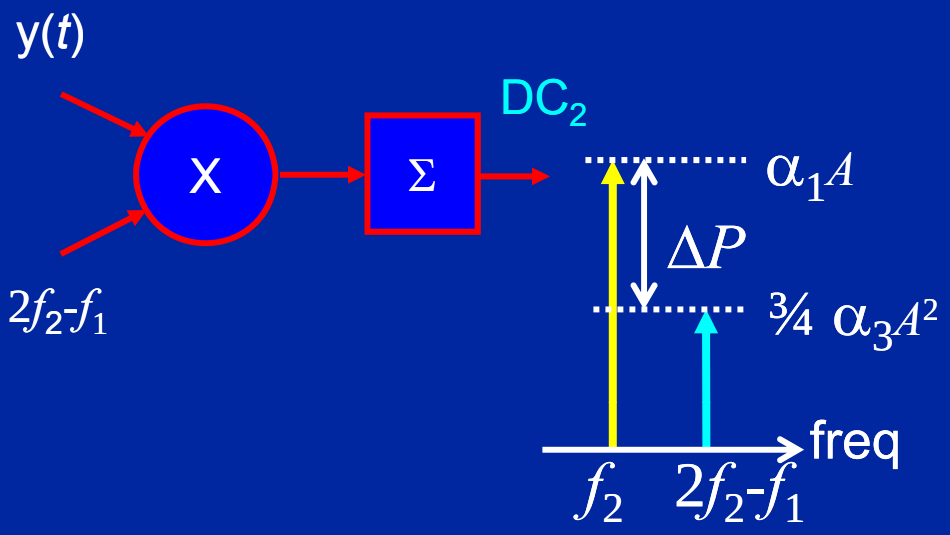


Actual Hardware Results

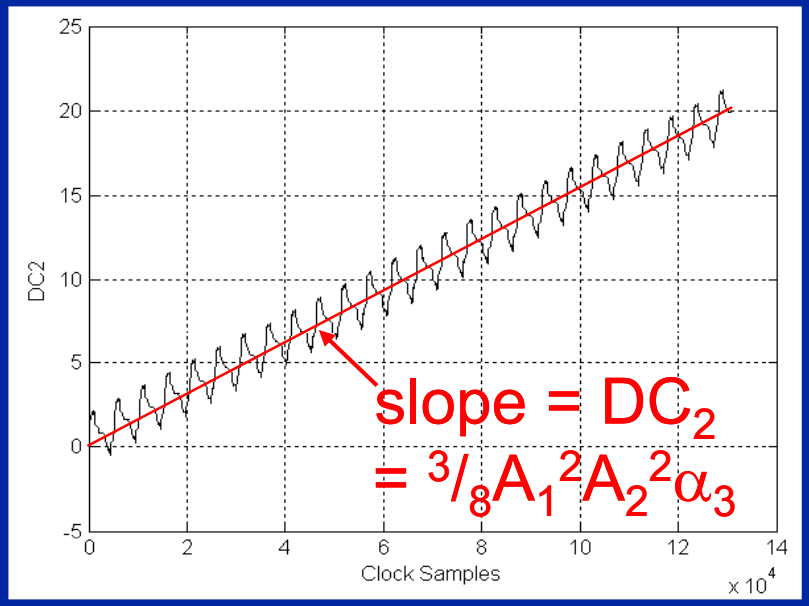


DC_2 Accumulator

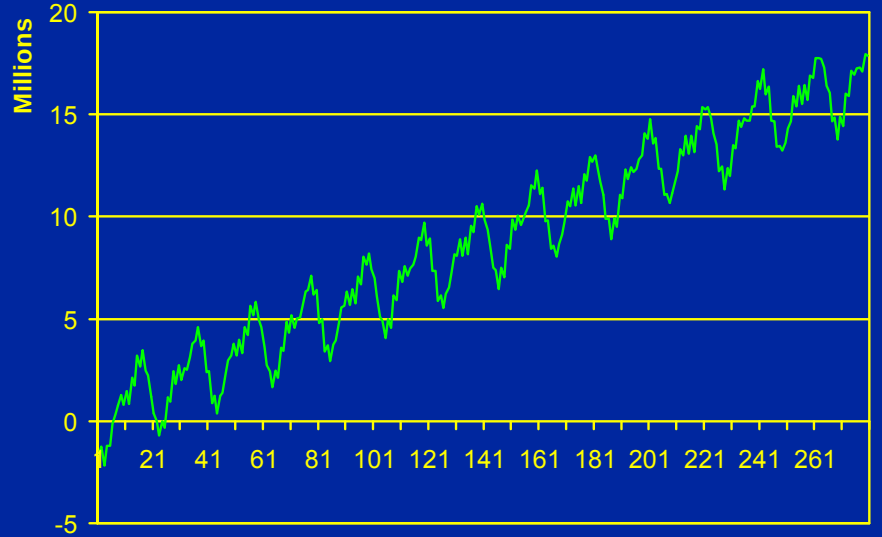
- $y(t) \times f_2 \Rightarrow DC_2 \approx {}^3/_8 A_1^2 A_2^2 \alpha 3$
- Ripple is bigger for DC_2
  - Test controller needed to obtain DC_2 at integral multiple of $2f_2\text{-}f_1$



Simulation Results



Actual Hardware Results

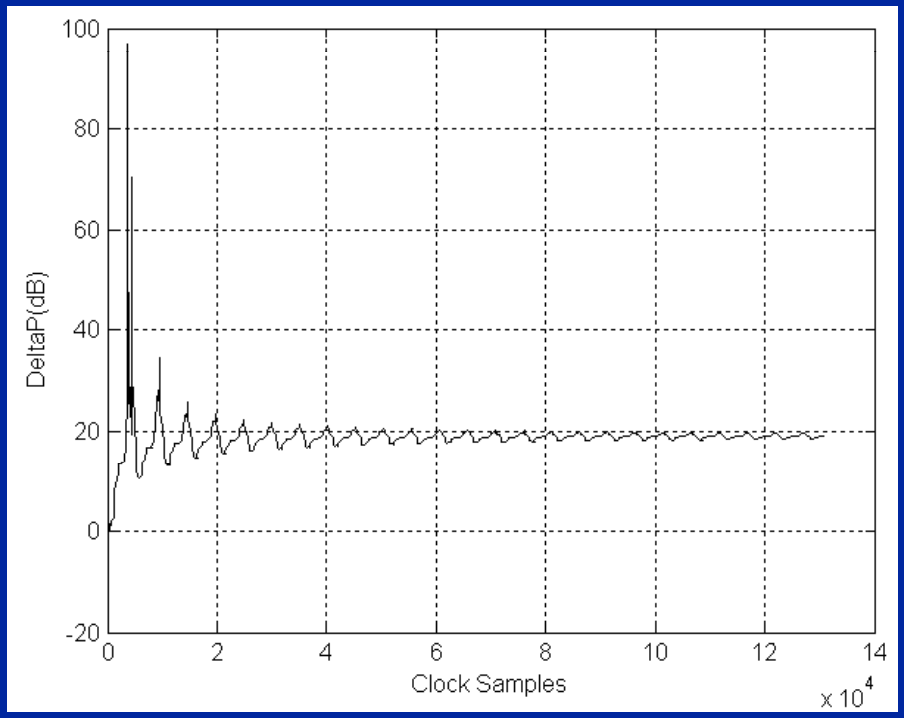


BIST-based ΔP Measruement

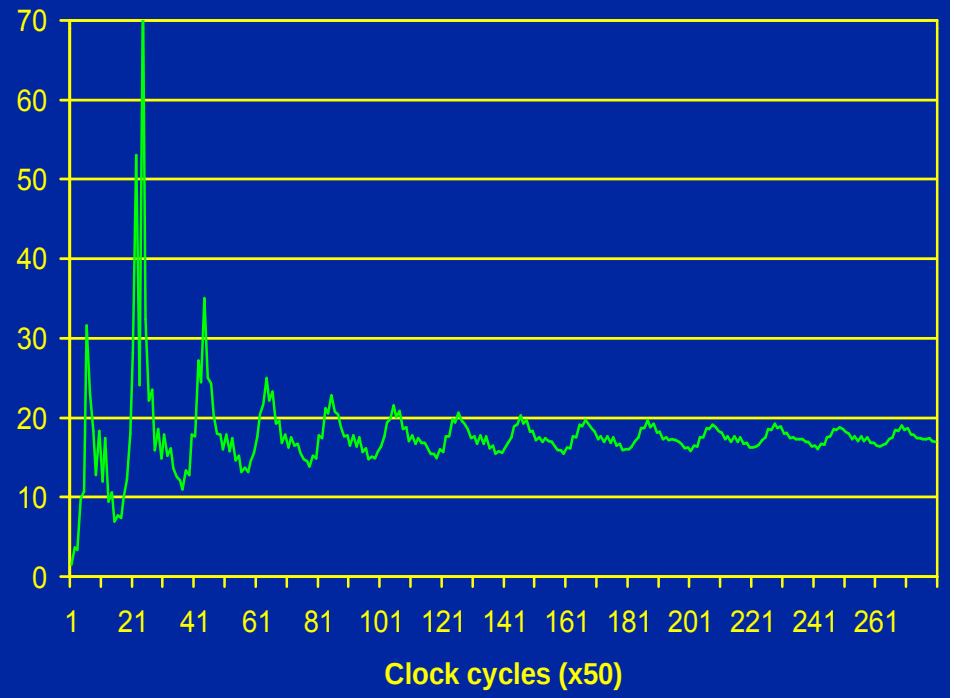
- DC_1 & DC_2 same proportionality to power at f_2 & $2f_2$-f_1
- Only need DC_1 & DC_2 from accumulators to calculate

  $\Delta P = 20 \log (DC_1) - 20 \log (DC_2)$

Simulation Results

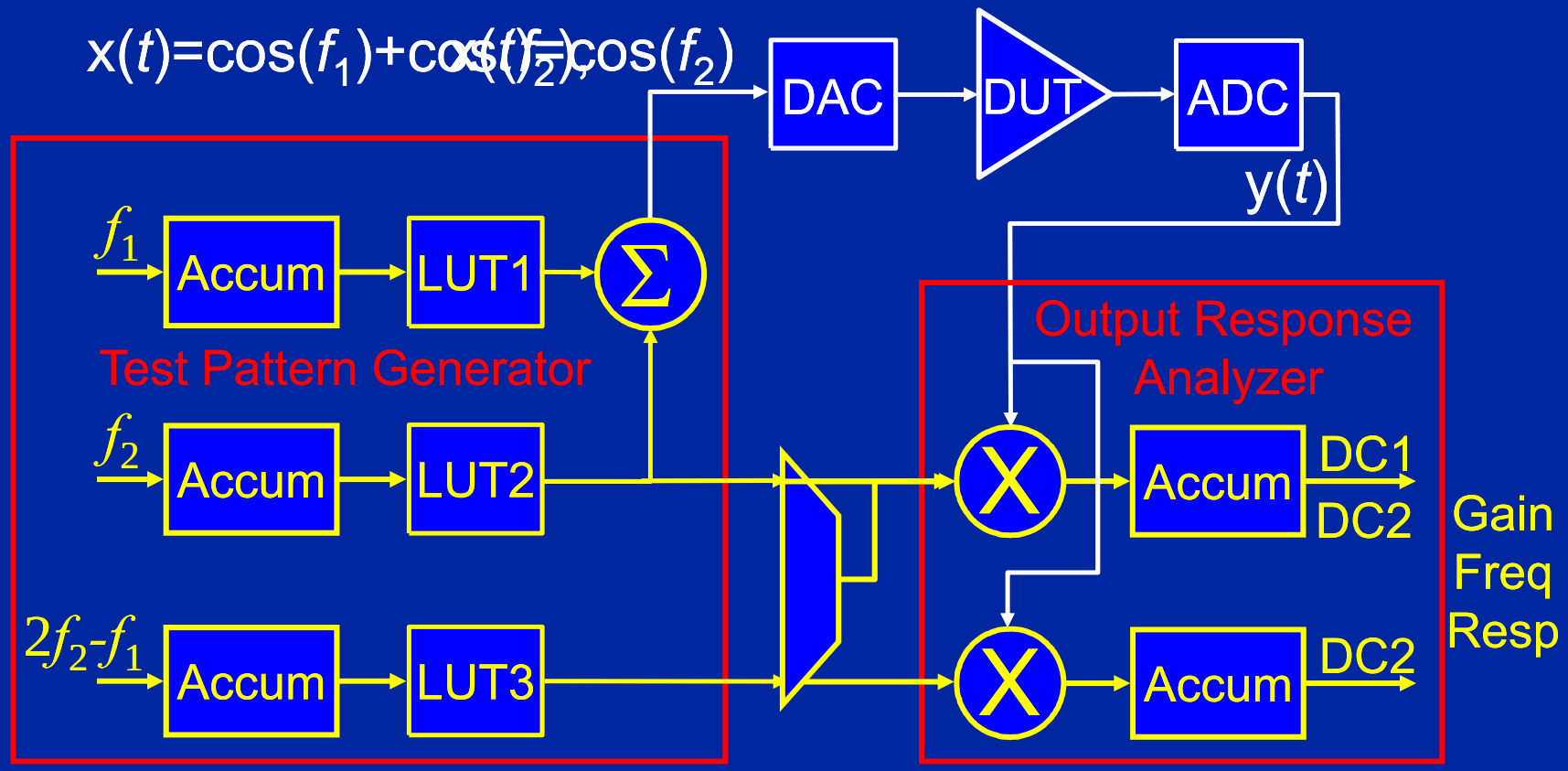


Actual Hardware Results



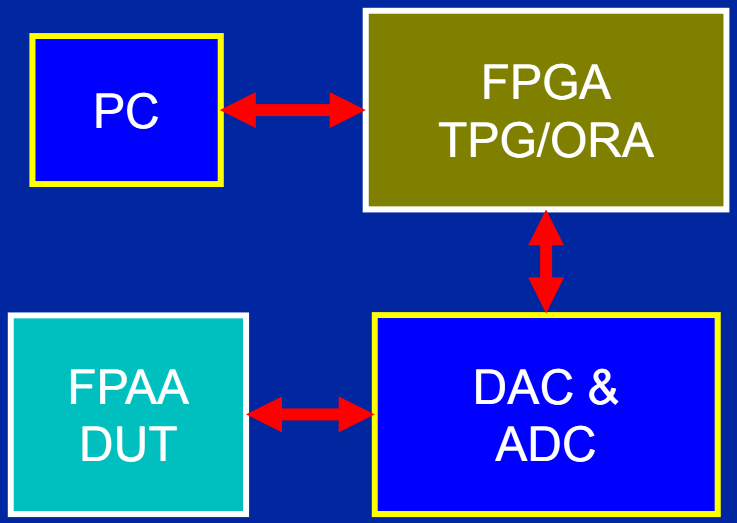
BIST Architecture

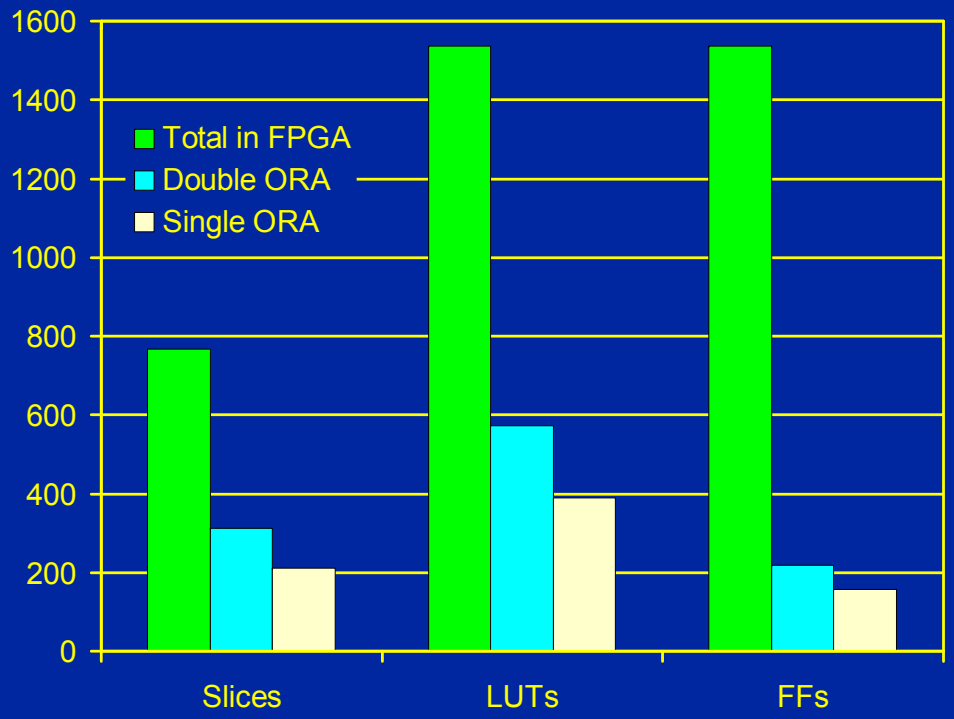
- BIST-based IP3 measurement
  - Reduce circuit by repeating test sequence for DC_2
- BIST-based Gain & Frequency Response is subset



Experimental Implementation of BIST

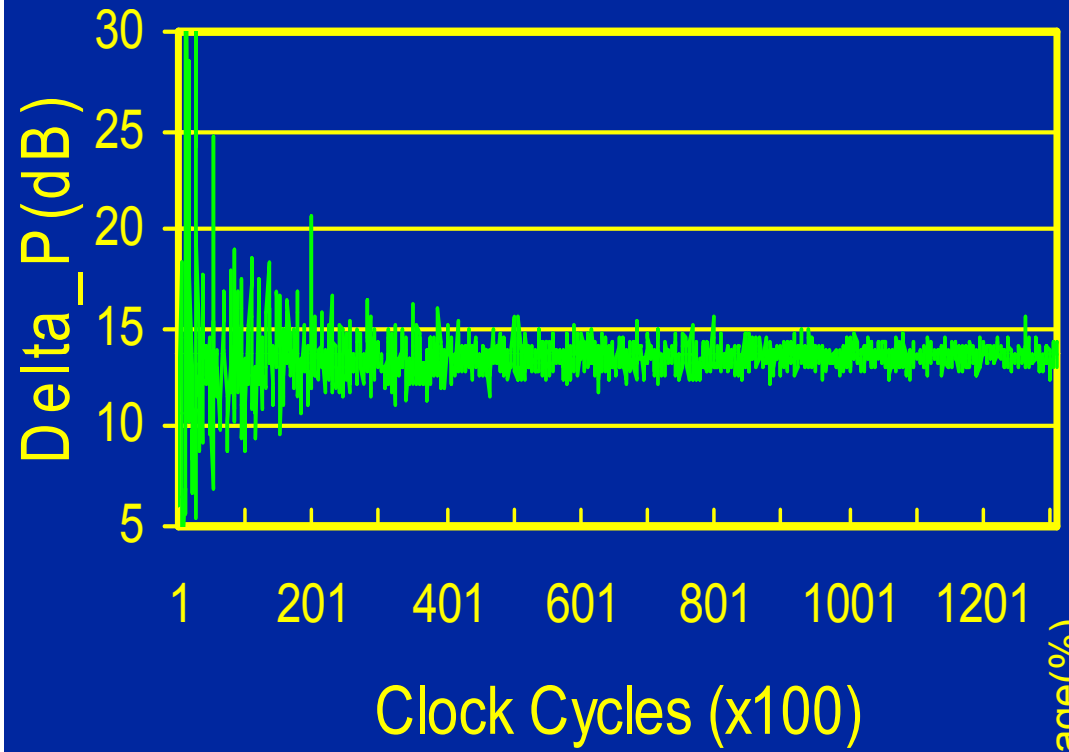
- TPG, ORA, test controller, & PC interface circuits
  - Three 8-bit DDSs and two 17-bit ORA accumulators
  - Implementation in Verilog
  - Synthesized into Xilinx Spartan 2S50 FPGA
- Amplifier device under test implemented in FPAA
- DAC-ADC PCB



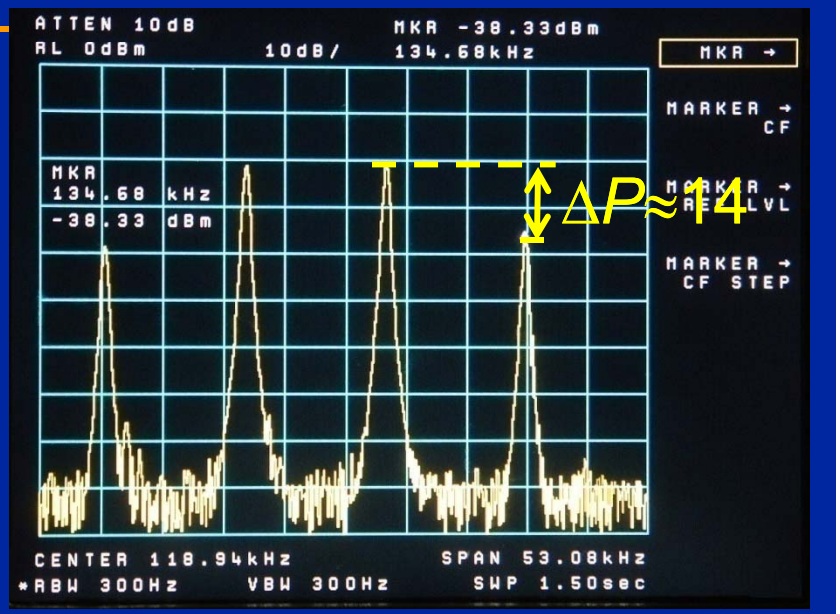


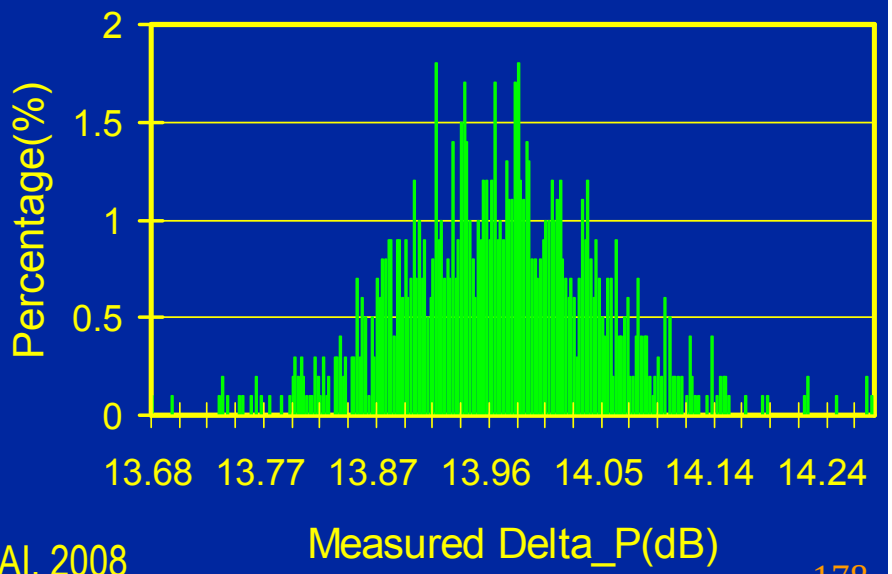
Hardware Results

BIST measures ΔP ≈ 14



Spectrum analyzer



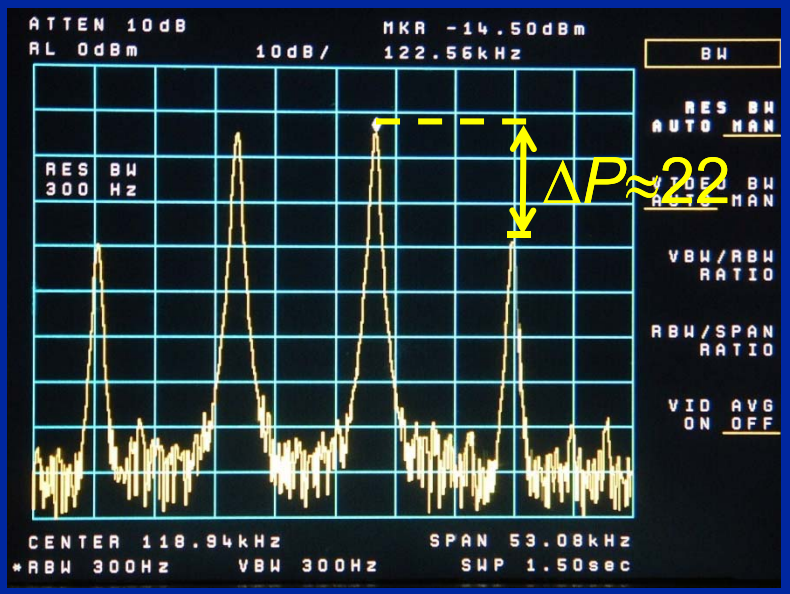


ΔP distribution for 1000 BIST measurements

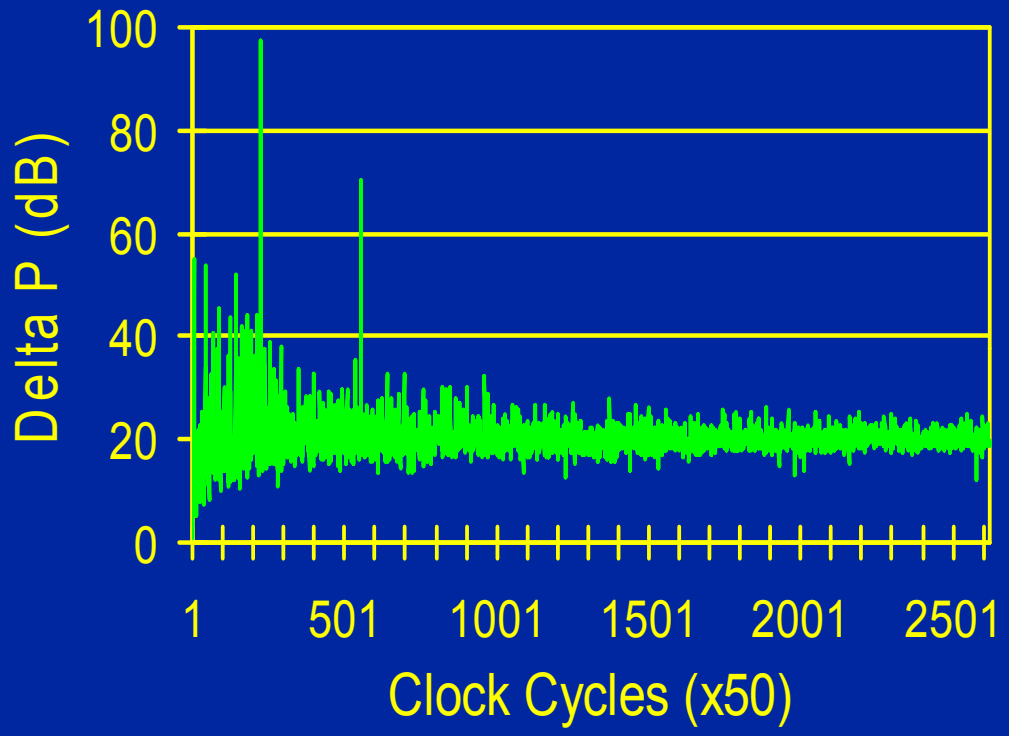
mean=13.97 dB, σ =0.082

More Hardware Results

Spectrum analyzer

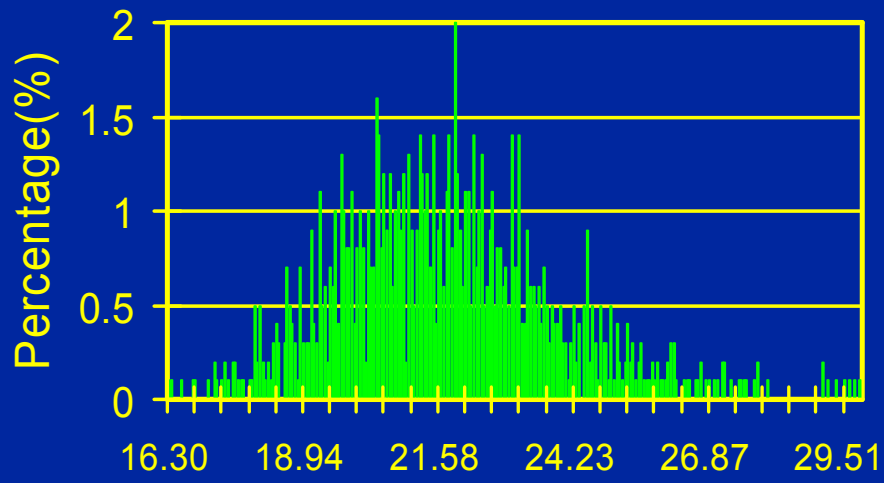


BIST measures ΔP ≈ 22



ΔP distribution for 1000 BIST measurements

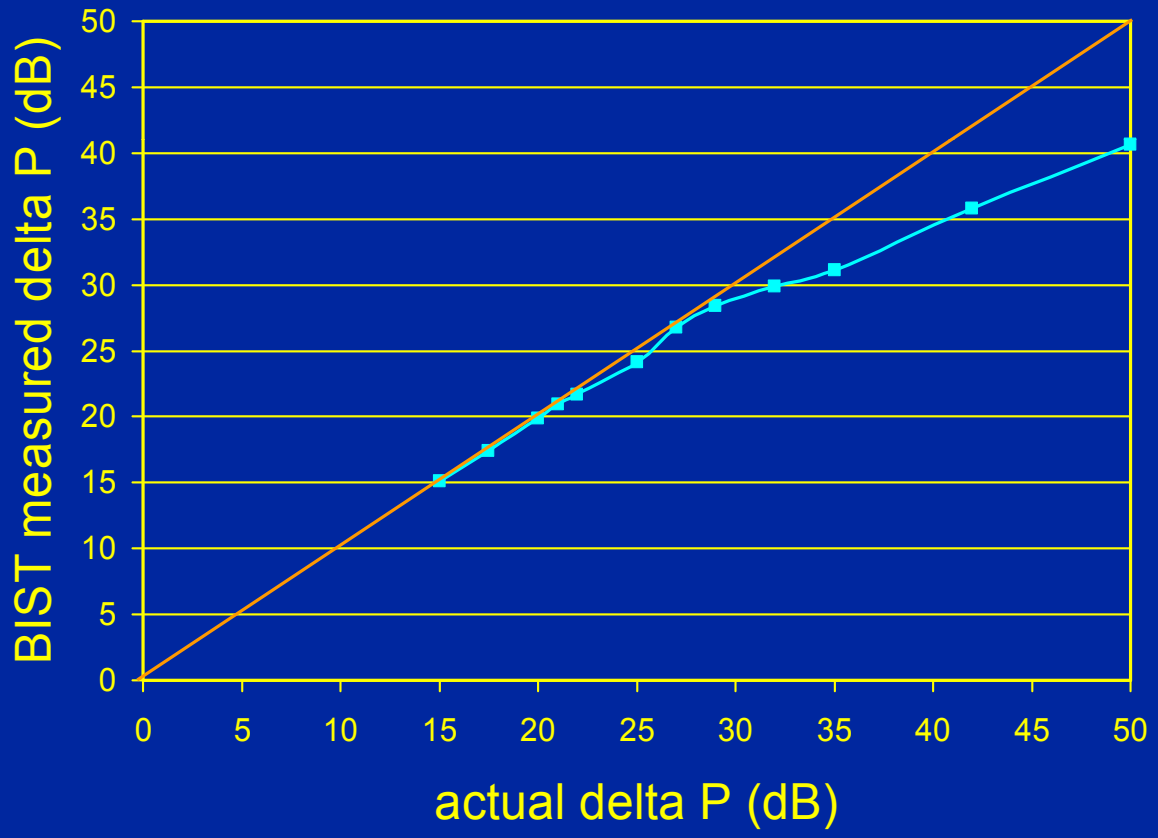
mean=21.7 dB, σ =2.2



Analog and mixed signal testing, FDAI, 2008

BIST IP3 Measurement Results

- Good agreement with actual values for ΔP < 30dB
- For measured ΔP > 30dB, the actual ΔP is greater
  - Good threshold since ΔP < 30dB is of most interest



Conclusion

- BIST-based approach for analog circuit functional testing
  - DDS-based TPG
  - Multiplier/accumulator-based ORA
- Good for manufacturing or in-system circuit characterization and on-chip compensation
  - Amplifier linearity (IP3)
  - Gain and frequency response
- Measurements with hardware implementation
  - Accurately measures IP3 $\leq$ 30dB
  - Measurements of IP3 > 30dB imply higher values